Mj. Int. J. Sci. Tech. **2008**, *2*(02), 308-319

Maejo International

Journal of Science and Technology

Full Paper

Theoretical analysis and design of double implanted MOSFET on 6H silicon carbide wafer for low power dissipation and large breakdown voltage

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Received: 2 February 2008/ Accepted: 26 April 2008 / Published: 1 May 2008

Abstract: This paper analyses the device structure of a 6H-SiC vertical double-implanted MOSFET (DIMOSFET) in order to provide a high breakdown voltage of about 10 kV and a low power dissipation for a rise in device temperature of 600 ^{o}C. Analysis of an 800 W power dissipation for stable device operation corresponding to this temperature rise shows optimum doping levels of the drift region lying between $5*10^{13}$ cm^{-3} and $5*10^{15}$ cm^{-3} for a breakdown voltage of 10 kV.

Keywords: silicon carbide, DIMOSFET, power dissipation

Introduction

Silicon Carbide (SiC) has been recently given renewed attention as a potential material for the high power and high frequency applications requiring high temperature operation. Some of the possible applications of SiC as a material of power electronic devices are for advanced turbine engines, propulsion systems, automotive and aerospace electronics and applications requiring large radiation damage resistance. Properties such as large breakdown electric field strength and large saturated electron drift velocity, small dielectric constant, reasonably high electron mobility, and high thermal conductivity make SiC attractive for fabrication of power devices with reduced power losses and die sizes. High thermal conductivity and breakdown electric field also suggest that integration of devices

made from SiC make possible higher packing densities and thus improvement in the current handling capability of these devices can be achieved. In spite of these advantages, research pertaining to SiC power devices and their practical application has been hampered by lack of reproducible techniques to grow semiconductor-quality single crystals and epilayers. However, recent developments in the growth of mono crystalline thin films of SiC by chemical vapour deposition and significant advancement in the growth of 6H-SiC single crystal boules, have stimulated a renewed interest in the SiC devices for a wide gamut of high-temperature and high-power device applications. Developments in the areas of the growth of the large area SiC bulk single crystal of 6H-SiC, improvement in the quality of SiC epilayers on Si and 6H-SiC substrates, high temperature ion implantation and doping of p and n types dopant, thermal oxidation reactive ion etching, discovery of ohmic contact materials, study of the electrical properties of grown and the doped films and their dependence on the temperature and advancements in the characterization techniques of the CVD-grown SiC films have made fabrication of high voltage SiC power devices a realistic possibility in the near future.

The SiC lattice consists of alternating planes of silicon and carbon items, and the stacking sequence of these planes defines different polytypes of the material identified by the repeat distance of the stacking sequence (e.g. 3C,4H & 6H). The lattice constant in the basal plane is virtually identical for all polytypes, but important electrical properties such as band gap energy, electron mobility and critical field differ significantly between the polytypes [1-5]. The high thermal and chemical stability of SiC makes certain types of fabrication difficult. Diffusion coefficients for dopant atoms are extremely low at the temperatures typically used for silicon device processing and for this reason selective doping of SiC are accomplished by ion implantation. Implant activation typically requires annealing at temperatures between 1000 and 1700°C. Chemical etching is impractical owing to the high chemical stability of SiC and selective etching is accomplished by reactive ion etching (RIE) using fluorinated gases.

SiC offers significant advantages for power electronics applications such as lamp ballasts, motor controls, medical electronics, automotive electronics, high-density high-frequency power supplies and smart-power application-specific integrated circuits. Hence, silicon carbide-based MOSFET can be used in high power application and hence MOSFETs require a high breakdown voltage. The one-step field plate termination can enhance the breakdown voltage to 910 V, embedded mesa termination can increase it to 1350 V and the embedded mesa with step field plating can give a breakdown voltage of 1100 V [6]. However, 6H-SiC DIMOSFETs in practice have attained a maximum blocking voltage of 760 V [7]. The specific on-resistance of the drift region of the MOSFET can be significantly reduced by enhancing the inversion channel mobility using pyrogenic re-oxidation annealing [8] thereby reducing the power dissipation. The present work aims at estimating theoretically the breakdown voltages, power dissipation and specific on-resistance at various doping levels by varying the drain voltage.

Status of SiC-Based MOSFETs

In late 1980s it had been observed that power silicon devices were approaching their theoretical limits [9,7] and that these limits could be significantly extended by fabricating power devices in the materials with higher breakdown electric fields, such as silicon carbide. For the majority of vertically

oriented carrier devices, the theoretical minimum value of the resistance-area product which is specific on-resistance under punch-through condition is:

$$R_{on-sp} = \left(\frac{3}{2}\right)^3 \frac{V_B^2}{\mu_n \varepsilon_S E_C^3} = \frac{3.375 V_B^3}{\mu_n \varepsilon_S E_C^3} \quad (1)$$

where $R_{on\text{-}sp}$ is the specific on-resistance in Ω cm^2, μ_n is the electron mobility perpendicular to the surface, ε_s is the permitivity of the semiconductor, E_C is the critical field for avalanche breakdown perpendicular to the surface and V_B is the designed blocking voltage of the drift region. Although it varies with doping, the critical field E_C in SiC is almost an order of magnitude higher than in silicon. Even allowing for the lower electron mobility, the specific resistance in SiC at a given blocking voltage is about 400 times that of the silicon.

The first MOSFETs in SiC were reported in late 1980s and the first power MOSFETs in 1994. The power devices were the vertical trench MOSFETs or UMOSFETs. UMOSFETs are attractive because the base and source regions are formed epitaxially without the need for ion implantation and associated high temperature annealing. In UMOSFETs, the MOS channel is formed on the sidewalls of trenches created by RIE. However, SiC UMOSFETs have been reported to have two serious problems: a) a high electric field occurs in the gate oxide caused by higher electric fields in the SiC drift region. This problem occurs at the trench corners leading to catastrophic failure of the gate oxide at higher drain voltages, thus restricting the maximum operating voltage to less than 40% of ideal breakdown voltage, and b) the low inversion layer mobility along the trench sidewalls results in high specific on-resistance, which nullifies the advantage of low drift region in SiC. By 1995, UMOSFETs fabricated on the carbon face of SiC had achieved the breakdown voltage of about 260V.

In 1997, Northrop Grumman Science and Technology Center introduced and fabricated the 4H-SiC UMOSFETs at the blocking voltages of 1.1 kV [10] and 1.4 kV[11]. In the same year it also introduced and fabricated the 4H-SiC DIMOSFETS at the blocking voltages of 900 V [12]. Also in the same year, Denso Corporation Japan introduced UMOSFET, which produced the blocking voltage of 450 V, specific resistance of 10.9 mΩcm^2 and $V_B^2/R_{on\text{-}sp}$ of 18.6 MW/cm^2 [13]. In 1998, Purdue University reported a SiC accumulation-channel UMOSFET with new structural features that shield the trench oxide from high electric fields in the blocking state. The new features consist of a p-type region formed in the trench bottom by self-aligned ion implantation and a thin n-type epilayer incorporated between the n-drift region and the p-type base [14].

A way to avoid the problem with oxide breakdown at the trench corners is to eliminate the trenches. This was accomplished in 1996 with the introduction of planar implanted DMOSFETs [15]. Since impurity diffusion is impractical in SiC, the base and source regions are formed by selective ion implantation using aluminum or boron for the p-type base and nitrogen for n+ source. Because p-type implants are conducted at temperatures between 1600 and 1700 ^{o}C, self-aligned implant process using polysilicon gates are not practical in SiC and realignment tolerances must be allowed between the base, the source and the gate features. Due to these disadvantages, the elimination of the trench corners resulted in a threefold improvement in device blocking voltage to 760 V. This blocking voltage was achieved using 6H-SiC [16].

Theoretical Analysis of Silicon Carbide High-Voltage DIMOSFET

DMOS transistors are common in silicon power device technology where the p-base and n+ source regions are formed by diffusion of impurities through a common mask opening. However, impurity diffusion is impractical in SiC because of the very low diffusion coefficients at any temperature. The Purdue group fabricated the first DMOS transistors in SiC using ion implantation to introduce dopants for the p-base and the n+ source [16]. The implanted DMOSFET requires that separate masks be used to define p-base and the n+ source. The construction is a vertical structure with a drift layer built on a highly conductive n+ layer. The n-drift region is designed to give the forward blocking capabilities as shown in Figure 1. The forward blocking capability is achieved by the pn junction between p-base region and n-drift region.

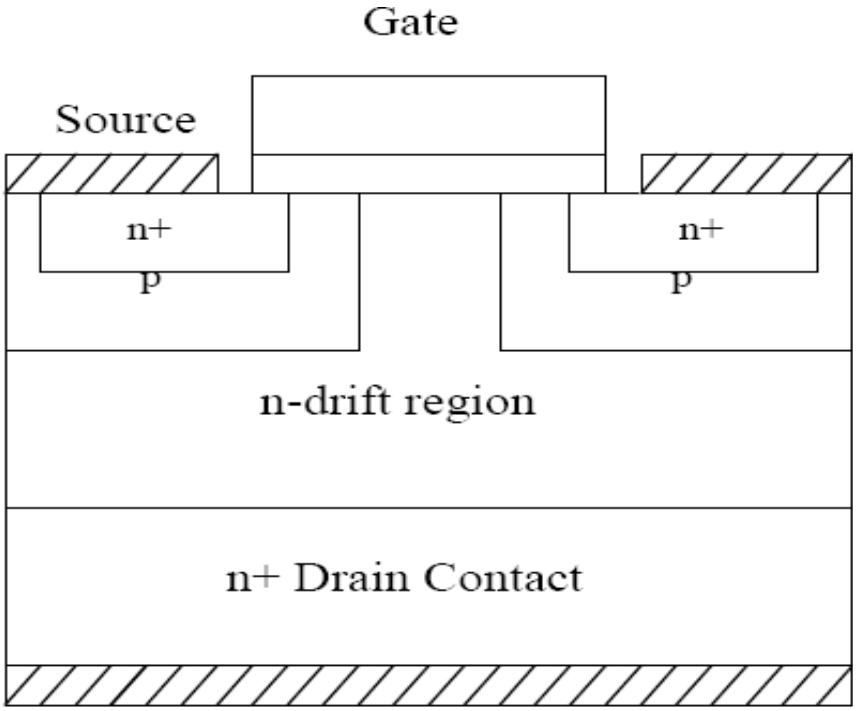

Figure 1. Structure of DIMOSFET

During the device operation, a fixed potential to the p-base region is established by connecting it to the source metal by the break in the n+ source region. By short-circuiting the gate to the source and applying a positive bias to the drain, the p-base/n-drift region junction becomes reverse-biased and this junction supports the drain voltage by the extension of depletion layer on both sides. However, due to the higher doping level of the p-base layer, the depletion layer extends primarily into the n-drift region. On applying the positive bias to the gate electrode, the conductive path between n+ source region and the n-drift region is formed. The application of positive drain voltage results in a current flow between drain and source through the n-drift region and conductive channel. The conductivity of the channel is modulated by the gate bias voltage and the current flow is determined by the resistance of various resistive components. The total specific on-resistance is determined as:

$$R_{on\text{-}sp} = R_{n+} + R_C + R_A + R_J + R_D + R_S \quad (2)$$

where $R_{on\text{-}sp}$ is the specific on resistance, R_{n+} is the contribution from the n+ source, R_C is the channel resistance, R_A is the accumulation layer resistance, R_J is the resistance from the drift region between the p-base regions due to JFET pinchoff action, R_D is the drift region resistance, and R_S is the substrate resistance.

In a power MOSFET, the blocking voltage is supported across the drift layer, and thus the drift-region resistance is considered to be the minimum possible theoretical limit for the on-resistance of a MOSFET. For an ideal DIMOSFET, the resistances associated with the n+ source, the n-channel, the accumulation region and the n+ substrate are assumed to be negligible and the specific on-resistance of the power MOSFET is determined by the drift region only. This assumption is not accurate at lower breakdown voltages where the drift region resistance R_D is comparable to the other resistive components and these resistances should be included in calculating $R_{on\text{-}sp}$. However, at higher breakdown voltages, R_D is significantly higher than other resistances and $R_{on\text{-}sp}$ can be approximated by R_D. The details of the device structure are shown in Figure 2.

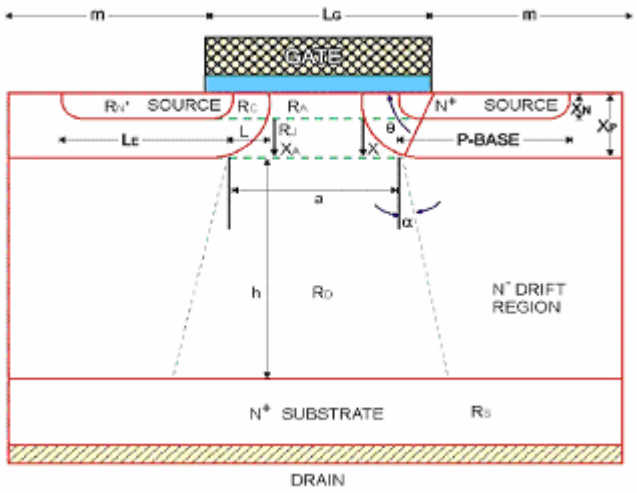

Figure 2. Cross section of power MOSFET

Basic device equations

Consider the depletion region between the p-base region and the n-drift region as a one-dimensional abrupt p-n junction. It can be shown that the doping level N_B (/cm^3) [17] that can support a given breakdown voltage V_B (V) and the depletion width W (cm) [18] at breakdown can be given as:

$$N_B = \frac{\varepsilon E_c^2}{2qV_B} \qquad (3)$$

and $$W = \frac{2V_B}{E_C} \qquad (4)$$

where q is the electron charge.

The specific on-resistance, $R_{on\text{-}sp}$ (Ω-cm^2) [19] of the drift layer to support V_B is

$$R_{on-sp} = \frac{W}{qN_B\mu_n^2} \qquad (5)$$

Substituting the values of eqs.(3) and (4) in eq.(5),

$$R_{on-sp} = \frac{4V_B^2}{\varepsilon E_C^3 \mu_n} \quad (6)$$

where ε is the permittivity (F/cm), E_C is the critical field of breakdown (V/cm) and μ_n is the electron mobility in cm^2/V-sec.

The equation connecting the breakdown electric field strength E_C on the doping level N_B for a pn diode of 6H-SiC has been derived. Based on these results the relationship between E_C and N_B was obtained [20]:

$$E_C = 1.95x10^4 \, xN_B^{0.131} V/cm \quad (7)$$

Eliminating E_C between eqs.(7) and (3),

$$N_B = \left(\frac{1.02x10^{15}}{V_B} \right)^{1.35} \quad (8)$$

This gives for R_{on-sp} from eq. (5),

$$R_{on-sp} = (5.93x10^{-9}) V_B^{2.5} \quad (9)$$

Finally the power dissipation P_D (W) [20] for the device for a 50% duty cycle can be evaluated using the equation,

$$P_D = \frac{1}{2}(J_{on}^2 A R_{on-sp} + J_L A V_B) \quad (10)$$

where J_{on} is the on-state current density in the linear region of (I_{DS}-V_{DS}) characteristics of the device in A/cm^2, and A is the device cross-sectional area in cm^2.

R_{on-sp} can be determined by the slope of I_{DS}-V_{DS} curve in the linear region. In our calculations we have set $J_{on} = \frac{I_{DS}}{A}$ to calculate the maximum power dissipation for a MOSFET, which is the maximum value corresponding to J_{on} for a given gate bias. Again $J_L << J_{on}$ and the second term in eq.(8) can be neglected. Hence eq.(10) can be written as:

$$P_D = \frac{1}{2}(J_{on}^2 A R_{on-sp}) \quad (11)$$

The exact equations for I_{DS} (current between drain and source), ρ_D (resistivity in drift region) and R_{on-sp} (specific on-resistance) [21-23] can be given by:

$$I_{DS} = \frac{Z\mu_n C_{ox}[2(V_G - V_T) - V_D^2]}{2L} \quad (12)$$

$$\rho_D = \frac{1}{\mu_n q N_B} \quad (13)$$

$$R_{on-sp} = \frac{\rho_D (L_G + 2m) \ln(1 + 4\tan 26^0) 10^{-4}}{\tan 26^0} \quad (14)$$

with

$$J_{on} = \frac{I_D}{200x10^{-8}} \text{ Ampere/cm}^2 \quad (15)$$

$$V_f = R_{on-sp} \, x \, J_{on} \quad (16)$$

where we have evaluated I_{DS} for V_{GS}= 40 volts, the threshold voltage V_T having been set equal to 1V as is usually the case. Z and L are the device dimensions shown in Figure 2, C_{OX} is the oxide

capacitance, and J_f and V_f are the forward current density and forward drop respectively. The rise in temperature of the device ΔT °K is proportional to P_D, the power dissipated:

$$\Delta T = \theta_{th} P_D \quad (17)$$

where θth is the thermal resistance associated with the device in Kelvin /Watt, its value depending on the state of the art device packaging technology. With today's technology θ_{th} is about 1°K/W giving

$$\Delta T = P_D \quad (18)$$

For all calculations we have used an average value of μ_n[24,20] of 530 cm^2/ V sec.

Calculations and related graphs

In calculating the current I_{DS} and power dissipation P_D, we have used the following parameters with the value quoted against each one of them: L_G=20μm, m=10 μm, Z= 10μm, L=3 μm, A=200x10^{-8} cm^2, $C_{ox}=\varepsilon_s/0.1$, V_G=40V, V_D=2V, V_T=1V, μ_n=530 cm^2/V-sec, h=30 μm, and a=15 μm. The set of the calculations were made on the basis of eqs. (1) to (15). By using these equations the following graphs (Figures 3-7) are plotted.

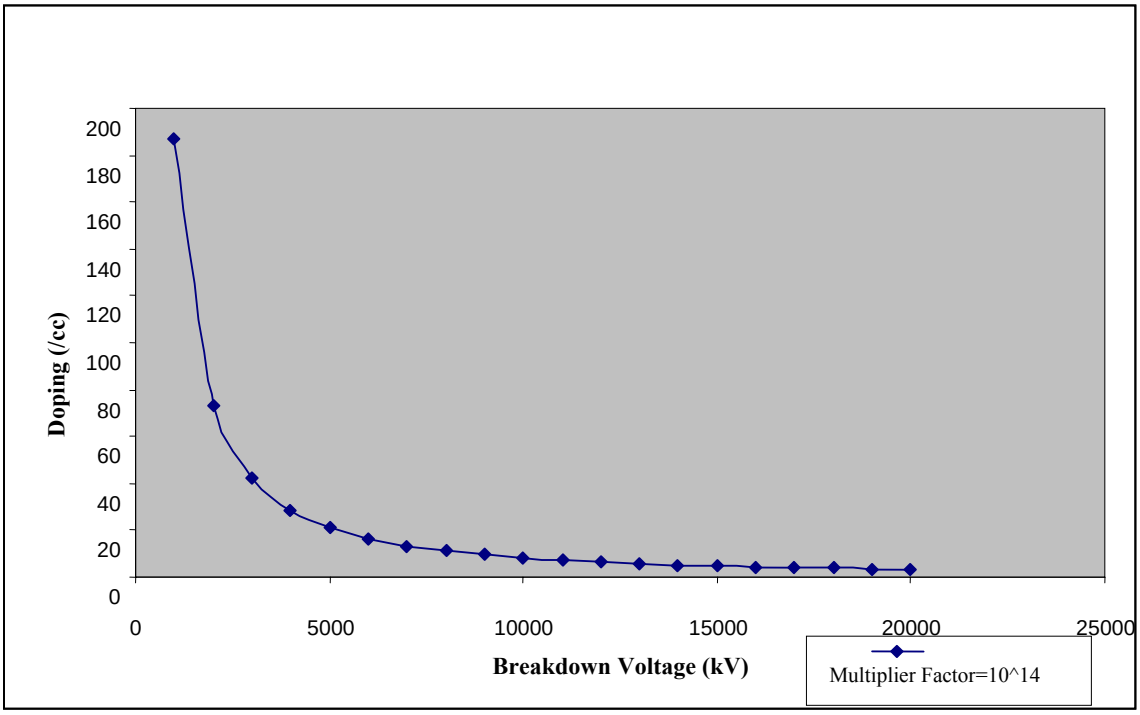

Figure 3. Plot of doping vs. breakdown voltage

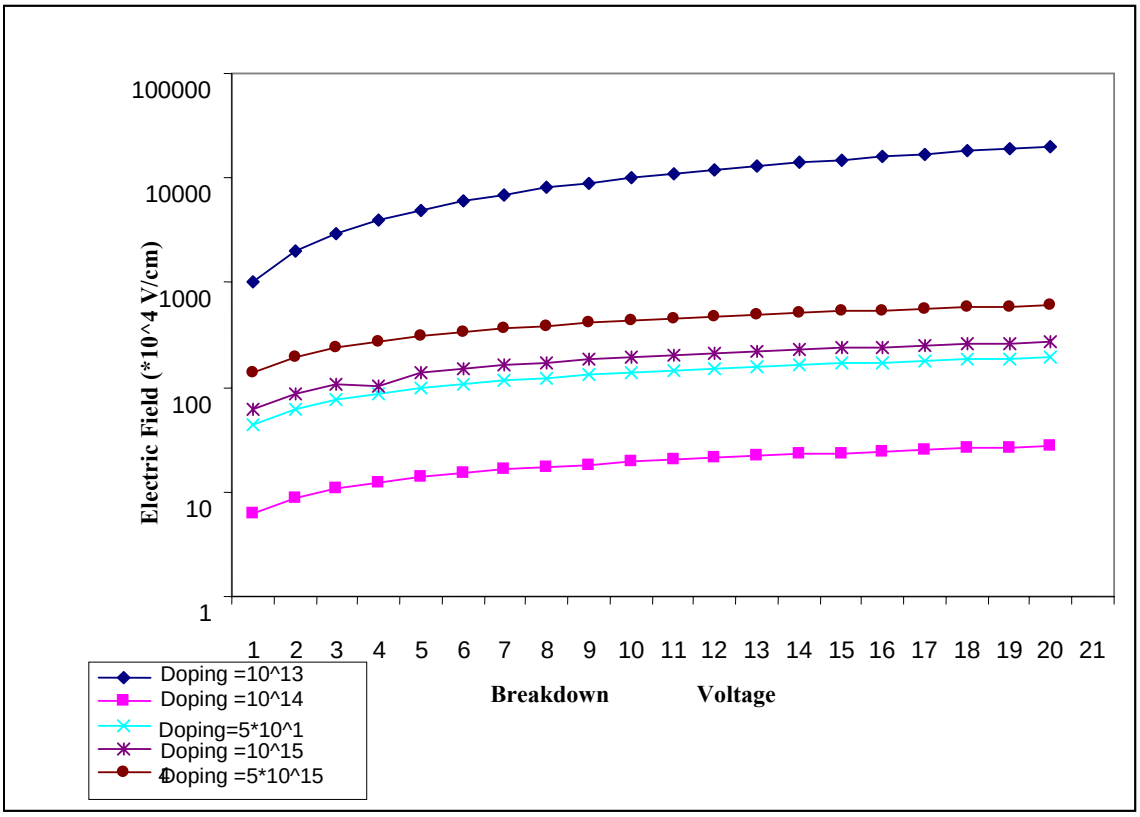

Figure 4. Plot of electric field vs. breakdown voltage

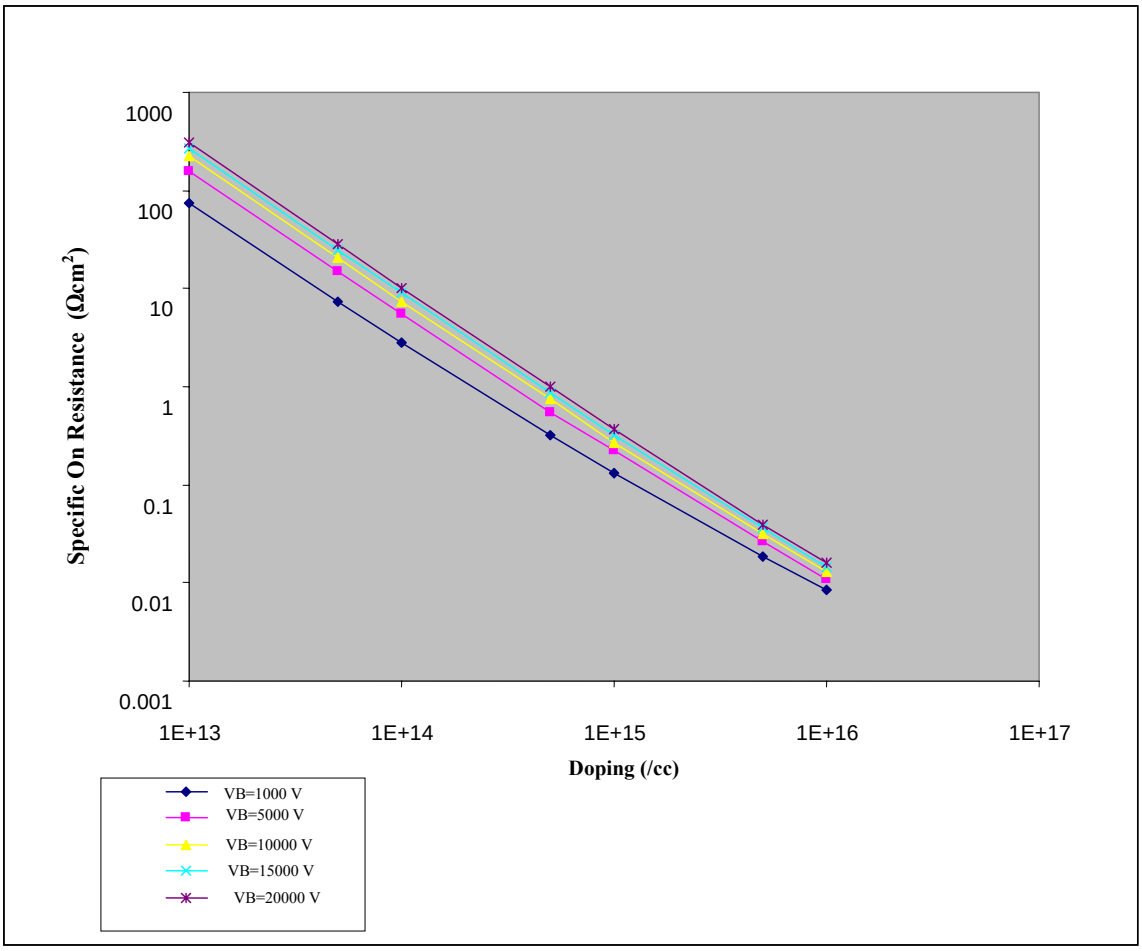

Figure 5. Plot of specific on-resistance vs. doping

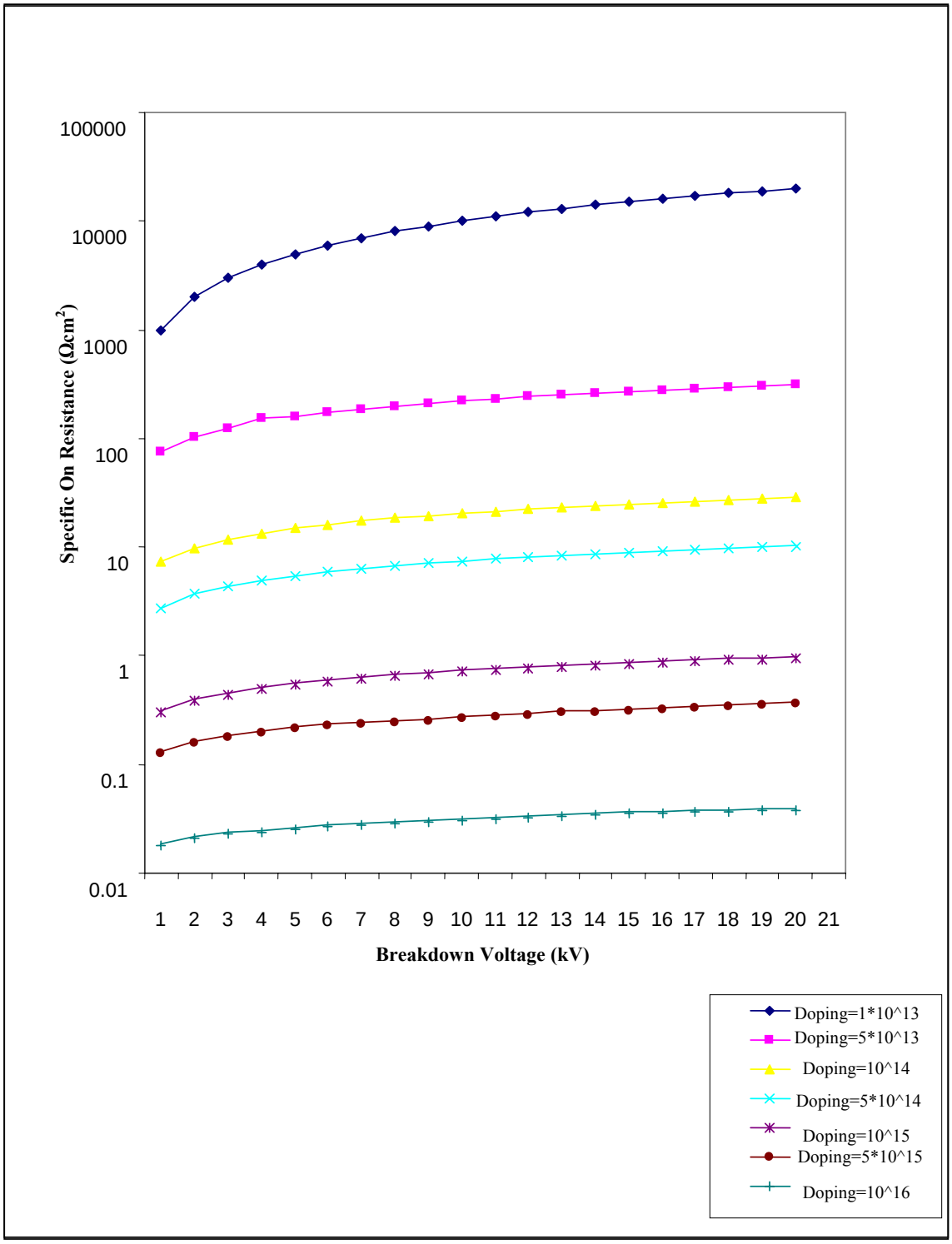

Figure 6. Plot of specific on-resistance vs. breakdown voltage

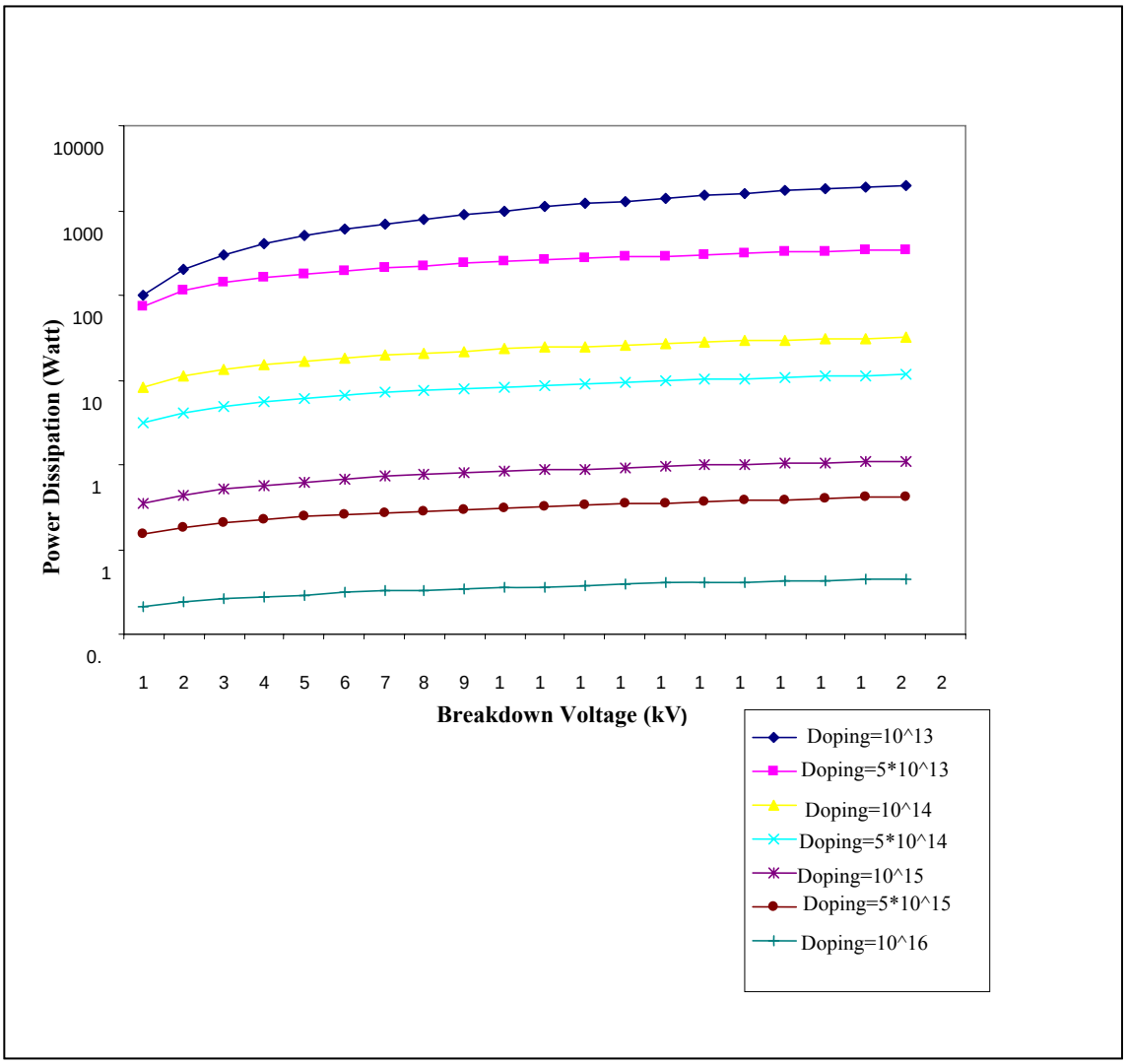

Figure 7. Plot of power dissipation vs. breakdown voltage

Results and Discussion

Having set the device dimension as above, we began by considering the graph of Figure 3 wherein it is seen that the high breakdown voltage ≅ 10 kV can be attained by using the low doping level of the order of 10^{15}/ cm^3 or less. However very low doping levels can give rise to a large parasitic drop across the drift region. Hence we needed to reduce this parasitic loss. We began with the design rule that a maximum value of the temperature rise ΔTmax of 600°C≅800 K for power dissipation is permissible with the latest packaging technology. This gives ΔTmax = P_{Dmax}=800 W. From Figure 7 we noted that at $V_B \geq 10$ kV, P_{Dmax} of 400 W can be attained with a doping level of $5*10^{13}cm^{-3}$. Making allowance for an increase in the $R_{on\text{-}sp}$ to twice its room temperature value over this range of the temperature rise for SiC power MOSFET, the safe margin would be to set $N_B = 5*10^{13}/cm^3$. At V_B = 10 kV and $N_B = 5*10^{13}/cm^3$, the $R_{on\text{-}sp}$ = 205 Ω-cm^2 (see Figure 6). Hence doubling of $R_{on\text{-}sp}$ at $N_B = 5*10^{13}/cm^3$ with rise in temperature could lead to doubling the level of permissible power dissipation to 800 W. This value of $R_{on\text{-}sp}$ can be checked from Figure 5, which gives plot of $R_{on\text{-}sp}$ vs. N_B for different values of V_B. Finally for V_B = 10 kV, $N_B = 5*10^{13}$/ cm^3, the critical field for breakdown, i.e.

E_c can be obtained from Figure 4 giving $E_c \cong 4.3*10^5$V/cm. Thus, apart from the device dimensions quoted above, we recommend a doping level of $5*10^{13}$/ cm^3 for an n-drift layer of 30μm thickness for the safe operation of a 6H-SiC power MOSFET with a breakdown voltage of 10 kV and a maximum rise in the device temperature of 600°C. However, in order to reduce parasitic loading effect of $R_{on\text{-}sp}$ of the drift region, it is recommended that either $5*10^{13}$/ cm^3 or 10^{15}/ cm^3 values for N_B can be safely used. Hence, the limit of N_B for a safe operation of 6H-SiC power MOSFET for 800W power dissipation in Figure 7 can be obtained by setting any value of N_B between $5*10^{13}$/cm^3 and 10^{15}/cm^3 for V_B =10 kV with E_c lying between $4.3*10^5$ V/cm and $4.3*10^6$ V/cm respectively.

Conclusions

The results of this paper are based primarily on the variation of specific on-resistance with temperature and its effect on the power dissipation using the concept of field independent mobility, which help to estimate the optimum doping levels of the drift region. The 6H-SiC power MOSFET designed in the paper has a low specific on-resistance, a high breakdown voltage of 10 kV, not-too-high electric field of Ec $\cong 10^6$V/cm, and a low power dissipation much less than a maximum limit of 800W. In our analysis we have used an average value of carrier mobility of 530 cm^2/V.sec. However, for still more accurate work it is advisable to use the field dependent mobility given by the equation: $\mu=\mu_0/ [1+ (\mu_0 E/ v_{sat})^{\beta}]^{1/\beta}$ where μ_0 = low field mobility of 530 cm^2/V.sec at $N_B = 10^{14}$/cm^3 with an electric field of about 1000 V/cm. However, experimental verification of such a device designed along the lines given in the paper remains to be done.

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