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Full Paper

Modelling and analysis of the effect of stacking chips with TSVs in 3D IC package encapsulation process

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Abstract: This paper presents the modelling and analysis of the encapsulation process for three-dimensional (3D) stacking-chip package with through-silicon via (TSV) integration. The fluid-structure interaction of the 3D stacking-chip package encapsulation was modelled by finite volume and finite element codes, which were solved separately. The effect of the increase in the number of stacking chips was analysed. The visualisation of the 3D stacking-chip package encapsulation process was presented at different filling times. The void formation around the stacking chips was identified for each case. The displacement and von Mises stress for the copper through-silicon vias were determined. The use of designed inlet-outlet heights in the integrated circuit package maintained the filling time of the encapsulation process and reduced the void of the packages as the number of stacking chips increased. The encapsulation model facilitated a clear visualisation and enhanced fundamental understanding of the design of a 3D integrated circuit encapsulation. The proposed analysis is expected to be a reference and guide in the design and improvement of 3D integration packages.

Keywords: 3D IC integration, through-silicon vias (TSVs), stacking chips, fluid-structure interaction, finite volume, finite element

INTRODUCTION

In the microelectronic industry, the trend of integrated circuit (IC) packaging is now towards miniaturisation and establishment of high-capacity and high-performance circuits for the rapid development of electronic devices. Three-dimensional (3D) integration [1] with through-silicon vias (TSVs) and 3D IC packaging [2] technologies enable package designers to accomplish their goals

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through stacking chips with TSVs. In 3D IC integration, thinned silicon chips and micro-size interconnection require reliable housings to maintain the device's reliability and protect them from the hazardous environment. The encapsulation process [3, 4] using epoxy-moulding compound (EMC) was widely used for various IC packages such as thin quad flat packages (TQFPs) [5, 6], thin profile small outline packages with wide side of lead on chip (TSOP II 54 L LOC) [7, 8], stacking-chip scale packages [9], mould array packages [10] and moulded underfills [11]. During the encapsulation process, the EMC is fed into the cavity through transfer moulding to encapsulate structures such as the silicon chips, wire bondings, solder bumps, paddles and passive components. An improper encapsulation process could lead to the reduction in package reliability and defects such as warpage, interconnector fracture, critical displacement or deformation of chips, solder bumps, TSVs and void formation.

Publications regarding TSVs report on studies of thermal stress, thermomechanical reliability, TSV filling, thinned stacking wafers, wafer-level bonding, TSV structures, strength evaluation, electro-migration performance, and stacking memory chips with TSVs. Lau [1] reported a considerable number of studies on TSV manufacturing and its hidden costs, focusing on TSVs for 3D integration. Equations for manufacturing cost per good die and TSV calculation were also discussed. Lau also addressed important recommendations and development of TSVs. Tu [2] reported the reliability challenges in the 3D IC packaging technology. Joule heating was a major concern, and electro-migration, stress migration and chip warpage under compressive stress were also considered challenging issues. Ko and Chen [12] conducted an excellent review on wafer-level bonding for 3D integration including advantages and disadvantages of the bonding technology. Wafer surface contamination, which was potentially due to the fabrication tool, was also a primary concern. High via density and better alignment could be achieved by silicon direct bonding technology and mechanical stability could be achieved by hybrid bonding.

An advantage of TSV technology is its application in diverse packages. Falat et al. [13] applied TSVs in microelectromechanical systems (MEMS) through the direct face-to-face chip-to-wafer bonding of an MEMS device and focused on the mechanical aspects of wafer-level packaging. They employed the finite-element method (FEM) on TSVs in substrates, considering temperature excursion, pressure during moulding, materials, and handling load effect on mechanical stress. Wang et al. [14] also proposed and developed an integrated MEMS probe card for wafer-level IC testing. The TSV composite structure utilised a silicon cantilever, guaranteeing better signal routing and low path resistance. In their study, no degradation was observed in the 100,000-cycle lifetime test.

The TSV technology is also applicable in complementary metal oxide semiconductors (CMOS). Gagnard and Mourier [15] reported that the fabrication of CMOS imager sensor has been directed towards 3D integration through bonding and via filling methods. The challenge in 3D integration is the mounting of the double-sided device on the interposers, which allows the connection of chips at various locations and sizes. Abouelatta-Ebrahim et al. [16] implemented the finite difference method in 2D and 3D TSV simulations and investigated the sensitive layer of CMOS inverters and stacking devices in 3D circuits.

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The IC packages became more compact and had higher performance and capacity as TSVs developed. Thinned wafers or silicon dies can now be stacked and their sizes reduced, as compared with those in conventional packaging. Ohba et al. [17] developed thinned wafer stacking and copper multilevel interconnects. They found that the increase in the number of stacking wafers was dependent on the degree of integration. The method developed was expected to be a low-cost and high-integration technology for post scaling. Burghartz et al. [18] reviewed the ultra-thin chip technology and its applications and presented a new challenge: the performance and integration density limitation in flexible electronics. Simulation modelling played a significant role in the TSV investigations. The FEM and modified virtual crack closure technique were utilised by Wu et al. [19] to investigate the delaminating behaviour in 3D stacking-chip package (SCP), focusing on the stacking copper bumps. They reported that the mesh density only affected the G value (energy release rate) at a specific element size.

Diverse TSV applications require different designs. Thus, various parameters should be considered and optimised in the TSV design process. However, the effects of TSV design parameters could reduce package reliability. Landani [20] analysed the effect of design parameters on the thermo-mechanical properties of TSVs and solder joints in 3D ICs and discovered that the underfill thickness and stiffness significantly affects the durability of the solder joint and that the diameter is an important factor for TSV durability. An increase in die thickness significantly decreased the durability of the solder joint and TSVs. Moreover, Landani [21] studied the effects of design parameters on the solid-liquid interdiffusion using FEM and considered the elastic-plastic behaviour in the finite element analysis. The most influential factors for interface stress and copper interconnectors were the silicon die and substrate thickness. Meanwhile, die thickness and underfill stiffness were identified as factors influencing the stress of solid-liquid interdiffusion bonds. The effect of the interconnection size and pitch on stress was smaller than that of die thickness.

The conductor resistance generally varies with the diameter. Therefore, this aspect should also be considered in TSV research. Kamto et al. [22] investigated resistance in single via and long via chains and reported that TSVs are more resistant to temperature cycling and less resistant to higher temperatures than to wire bonding. A different TSV design, advanced clamped-TSV, was developed by Shen et al. [23] and was used in 3D chip-to-chip/wafer packaging. This cost-effective TSV fabrication process does not have layer deposition and photo processes. The clamped-TSV yielded lower thermal stress and higher bonding reliability for stacked bonding compared with the typical TSV design. The electromigration performance of TSVs was studied by Tan et al. [24] using FEM on a different pattern of top metallisation. According to them, the thermomechanical stress, which behaves asymmetrically, is more dominant over electromigration than the current density and failure modes of electromigration in TSVs.

Package reliability has always been a concern among researchers in the microelectronic industry. To achieve their goals, these researchers consider many aspects in the research and development of TSV technology. Wu et al. [25] employed FEM and a four-point bending test to evaluate the strength of silicon dies covered with polymer films. They found that polymer films enhanced the strength of 10 layers of 3D stacking dies during the fabrication process; the structure had no die cracks during thermal cycling. Tsai and Chen [26] proposed a new point load test on the

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different die surfaces to evaluate the strength of silicon dies. The point load test provided more data than the four- and three-point tests when considering the effect of surface roughness on silicon die.

The various IC applications of TSV technology and the diverse applications of the encapsulation process in different packages were reported [3-11]. However, the investigation of the encapsulation process in 3D IC packages considering TSVs and structural analysis is still rarely reported in the literature. The encapsulation process of stacking-die packages reported by Moon et al. [4] and Abdullah et al. [9] mainly focused on the fluid flow analysis and the interconnection of their IC packages using wire bonding instead of TSVs. Hence, the present study considers the 3D IC package with stacking chips connected by TSVs. It also focuses on the 3D modelling of the SCP and the effect of inlet-outlet heights during the encapsulation process. FLUENT 6.3 and ABAQUS 6.9 are utilised to perform the fluid and structural analyses. The effects of the EMC flow behaviour in the stacking chips and the stress and displacement on the TSVs are also investigated.

PROBLEM DESCRIPTION

The major issues in IC packaging are the IC package malfunction due to cracks and fractures at the interconnector, the critical displacement of the silicon chips and interconnector, and the void formation. Factors that influence the package quality during the encapsulation process include package design, material selection and process control. The design of the physical characteristics of the IC package and moulding parameters, such as inlet and outlet gates, orientation of stacking chips, number of stacking chips, solder bump standoff height and package size, may affect the fluid flow, filling time and void formation in the encapsulation [6]. Improper selection of EMC materials [11] may also cause void formation, delamination and shrinkage of compound. Improper process control such as that of moulding pressure and temperature [27] may also affect the package reliability. Figure 1 illustrates a schematic diagram of 10 layers of the SCP with TSVs. Generally, the increase in the number of stacking chips also increases the package volume. Therefore, a longer filling time is required and void formation may occur in the package, especially at the narrow space between stacking chips. Thus, the moulding parameters should be properly designed to maintain package reliability and reduce manufacturing cost. The present study mainly focuses on the effect of the number of stacking chips (2-6 stacking chips) on the fluid flow and structural deformation of the interconnector. Other parameter issues are considered as beyond the scope of the study. The designed inlet (h_{inlet} = 0.5t) and outlet (h_{outlet} = 0.25t) heights are applied in the package design, where t is the thickness of the package. The current study investigates five cases, namely cases 1–5 for packages with 2, 3, 4, 5 and 6 stacking chips respectively. The EMC flow behaviour is modelled using the Castro-Macosko model which was programmed using Microsoft VISUAL STUDIO.NET [6] and compiled with FLUENT code using user-defined functions. The force induced by the viscous fluid on the silicon chips and TSVs is used in the structural analysis in the ABAQUS code.

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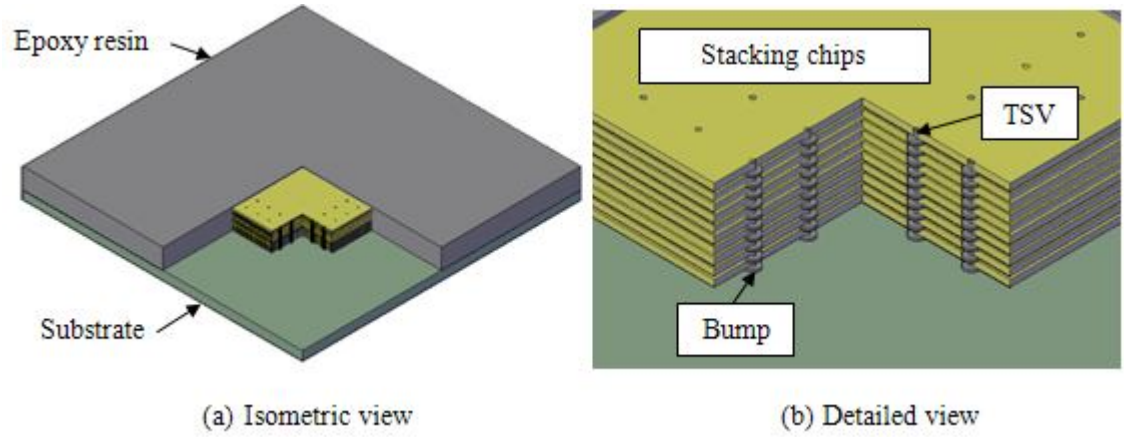

Figure 1. Isometric and detailed views of SCP

METHODS

Nomenclature

A_1, A_2	Pre-exponential factors	1/s
B	Exponential-fitted constant	Pa.s
C_1,C_2	Fitting constant	-
C_P	Specific heat	J/kg-K
E_1,E_2	Activation energies	K
E	Elastic modulus	GPa
F	Front advancement parameter	-
$\vec{g}$	Gravitational acceleration	m/s^2
k	Thermal conductivity	W/m-K
K_1, K_2	Rate parameters described by an Arrhenius temperature dependency	1/s
m_1, m_2	Constants for the reaction order	-
n	Power law index	-
p	Pressure	Pa
T	Temperature	K
t	Time	s
T_b	Temperature-fitted constant	K
u	Fluid velocity component in x-direction	mm/s
v	Fluid velocity component in y-direction	mm/s
w	Fluid velocity component in z-direction	mm/s
x, y, z	Cartesian coordinates	-
Greek letters		
α	Conversion of reaction	-
α_{gel}	Degree of cure at gel	-
ΔH	Exothermic heat of polymerisation	J//kg
η	Viscosity	Pa.s
η_0	Zero shear rate viscosity	Pa.s

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ρ	Density	kg/m^3
ρ_s	Solid density	kg/m^3
$\overleftrightarrow{\sigma}$	Recoverable stresses	Pa
τ	Shear stress	Pa
$\dot{\gamma}$	Shear rate	1/s
τ^*	Parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve	Pa
ν	Poisson ratio	-

Governing Equations

In fluid flow analysis the continuity, Navier-Stokes, and energy equations are accounted for in describing the EMC flow by considering the fluid incompressible. The equations are solved in the simulation (FLUENT) as follows.

Continuity equation:

$$\frac{\partial u}{\partial x}+\frac{\partial v}{\partial y}+\frac{\partial w}{\partial z}=0 \tag{1}$$

The motion of the fluid flow in the encapsulation process is described by Navier-Stokes equation [6], expressed in terms of x, y and z directions:

x-direction

$$\frac{\partial u}{\partial t}+u\frac{\partial u}{\partial x}+v\frac{\partial u}{\partial y}+w\frac{\partial u}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial x}+\left[\frac{\partial}{\partial x}\left(\eta\frac{\partial u}{\partial x}\right)+\frac{\partial}{\partial y}\left(\eta\frac{\partial u}{\partial y}\right)+\frac{\partial}{\partial z}\left(\eta\frac{\partial u}{\partial z}\right)\right] \tag{2}$$

y-direction

$$\frac{\partial v}{\partial t}+u\frac{\partial v}{\partial x}+v\frac{\partial v}{\partial y}+w\frac{\partial v}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial y}+\left[\frac{\partial}{\partial x}\left(\eta\frac{\partial v}{\partial x}\right)+\frac{\partial}{\partial y}\left(\eta\frac{\partial v}{\partial y}\right)+\frac{\partial}{\partial z}\left(\eta\frac{\partial v}{\partial z}\right)\right] \tag{3}$$

z-direction

$$\frac{\partial w}{\partial t}+u\frac{\partial w}{\partial x}+v\frac{\partial w}{\partial y}+w\frac{\partial w}{\partial z}=-\frac{1}{\rho}\frac{\partial p}{\partial z}+\left[\frac{\partial}{\partial x}\left(\eta\frac{\partial w}{\partial x}\right)+\frac{\partial}{\partial y}\left(\eta\frac{\partial w}{\partial y}\right)+\frac{\partial}{\partial z}\left(\eta\frac{\partial w}{\partial z}\right)\right] \tag{4}$$

The temperature of fluid flow in the encapsulation process is described using the energy equation [6]:

$$\rho C_p\left(\frac{\partial T}{\partial t}+u\cdot\nabla T\right)=\nabla\left(k\nabla T\right)+\Phi, \tag{5}$$

where the source term Φ is defined as:

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$$\Phi = \eta \dot{\gamma}^2 \tag{6}$$

$$\dot{\gamma} = \sqrt{\left(\frac{\partial u}{\partial x}\right)^2 + \left(\frac{\partial v}{\partial y}\right)^2 + \left(\frac{\partial w}{\partial z}\right)^2} \tag{7}$$

The viscosity of the EMC during encapsulation is modelled by the Castro-Macosko model [5, 28-30] with curing effect (Kamal's equation) in the current study. The viscosity changes and reactions of the encapsulant are influenced by the temperature in the process. The encapsulant material is assumed to be a general Newtonian fluid. The Castro-Macosko model is used to predict the relationship between viscosity and degree of polymerisation and describes the viscosity of the encapsulant material:

$$\eta(T,\dot{\gamma}) = \frac{\eta_0(T)}{1+\left(\frac{\eta_0 \dot{\gamma}}{\tau^*}\right)^{1-n}} \left(\frac{\alpha_g}{\alpha_g - \alpha}\right)^{C_1 + C_2 \alpha} \tag{8}$$

with

$$\eta_0(T) = B \exp\left(\frac{T_b}{T}\right) \tag{9}$$

where B is an exponentially fitted constant, T is temperature, T_b is a temperature-fitted constant, n is the power law index, η_o is the zero-shear viscosity, $\dot{\gamma}$ is the shear rate, τ^* describes the transition region between zero-shear rate and power law region of the viscosity curve, α is the conversion of reaction, α_g is degree of cure at gel, and C_1 and C_2 are fitting constants.

Kamal's equation [5, 28-30] is coupled with the Castro-Macosko model in the current study. The chemical conversion of EMC occurs during the IC encapsulation process. The cross-linking reactions of the EMC material increase its viscosity and influence the conversion of the reaction (α). The consideration of the curing effect, which is described by Kamal's equations, is important in describing the EMC curing behaviour in IC encapsulation process. The rate of chemical conversion of the EMC in this model is predicted as follows:

$$\frac{d\alpha}{dt} = \left(k_1 + k_2 \alpha^{m_1}\right)(1-\alpha)^{m_2} \tag{10}$$

$$k_1 = A_1 \exp\left(-\frac{E_1}{T}\right) \tag{11}$$

$$k_2 = A_2 \exp\left(-\frac{E_2}{T}\right) \tag{12}$$

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where α is the degree of conversion, A_1 and A_2 are Arrhenius pre-exponential factors, E_1 and E_2 are activation energies, m_1 and m_2 are reaction orders, T is the absolute temperature, and k_1 and k_2 are rate parameters described by Arrhenius temperature dependency.

The volume of fluid (VOF) model [6] is applied to treat the two distinct phases (air and EMC). It is used to calculate the interface tracking of the encapsulant/air interface in the analysis. The computational domain consists of both the encapsulant and air regions. As time increases, the encapsulant phase increases and the air phase decreases. The melt front over time is governed by the following transport equation:

$$\frac{dF}{dt} = \frac{\partial F}{\partial t} + u\frac{\partial F}{\partial t} + v\frac{\partial F}{\partial t} + w\frac{\partial F}{\partial t} - \left\{ \frac{\partial^2 F}{\partial x^2} + \frac{\partial^2 F}{\partial y^2} + \frac{\partial^2 F}{\partial z^2} \right\} = 0 \tag{13}$$

where F is the fraction of the cell volume occupied by liquid. In the simulation result of flow front advancement (as shown later in Figure 11), the cell (mesh element) that contains only the resin is represented in red (F=1), and the cells without resin are represented in white (F=0). Values between 0 and 1 (0<F<1) in the 'interface' cells are referred as the EMC melt front.

In the structural analysis, the momentum equation [31] used in FEM based (ABAQUS) for solving the structural deformation is as follows:

$$\rho_s \left(\frac{\partial \vec{u}}{\partial t} + \vec{u}.\nabla \vec{u} \right) = -\nabla \overleftrightarrow{\sigma} + \rho_s \vec{b} \tag{14}$$

where ρ_s is density of the solid, $\vec{u}$ is velocity of the solid in x-, y- and z-axes, $\vec{\sigma}$ is recoverable stress, and $\vec{b}$ is mass force.

Simulation Model Description

Generally, the increase in package thickness and volume is attributed to the increase in the number of stacking chips. According to a previous study [6], the rise in the number of inlet gates significantly raises the cavity pressure, reduces the air trap and shortens the filling time in the thin quad flat package (TQFP) encapsulation. However, the present study considers a single inlet and outlet using designed inlet-outlet heights, which are applicable to packages with different numbers of stacking chips. The inlet (h_{inlet}) and outlet (h_{outlet}) heights of the mould were designed (Table 1) to be 50% and 25% of the mould thickness respectively, with a width (w) of 4 mm each. The mould thickness (t) is illustrated in Figure 2, together with the top, front and detailed views of the package with six stacking chips and TSVs. The gap between the mould wall and the top surface of the silicon chips was set to h_1 = 0.1 mm for all cases, as shown in Figure 3. The dimension of the 3D model [19] of the SCP is presented in Table 2.

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Table 1. Detail of SCPs with different numbers of stacking chips under study

Case	No. of stacking chips	Mould thickness, t (mm)	h_{inlet} (= 0.5t) (mm)	h_{outlet} (= 0.25t) (mm)
1	2	0.405	0.2025	0.1013
2	3	0.575	0.2875	0.1438
3	4	0.745	0.3725	0.1863
4	5	0.915	0.4575	0.2288
5	6	1.085	0.5425	0.2713

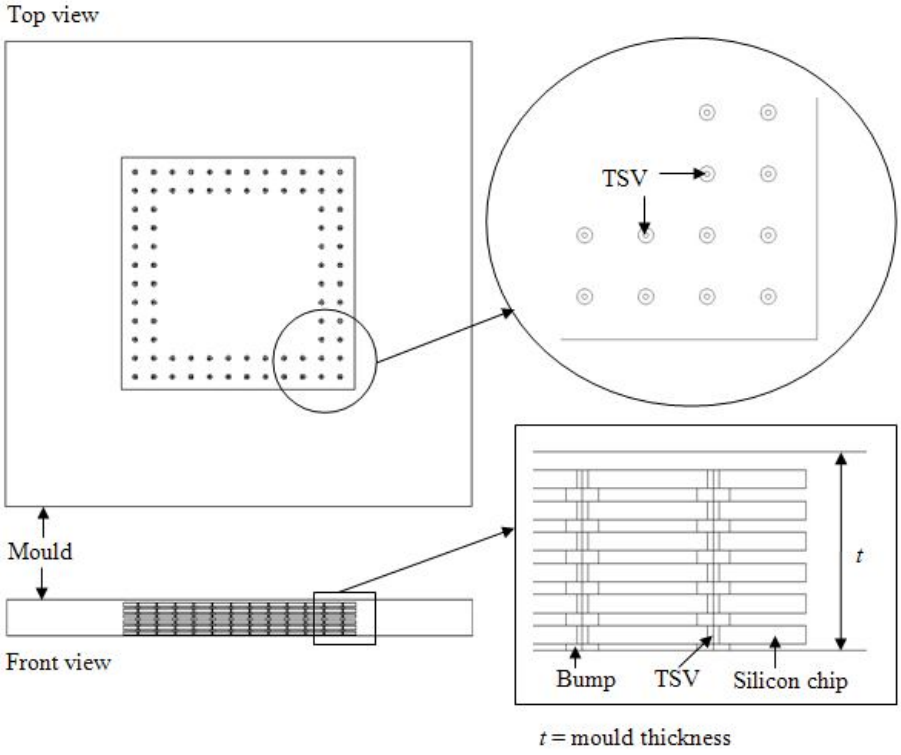

Figure 2. Top view, front view and detailed views of SCP (six chips)

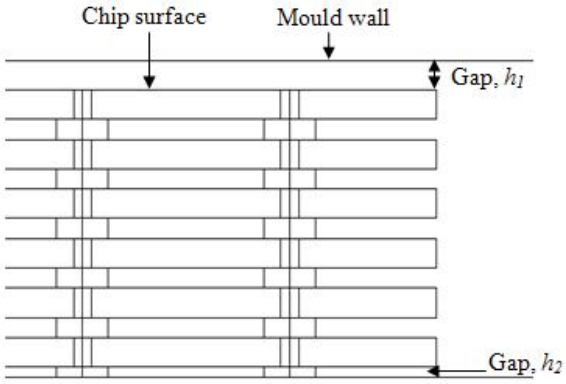

Figure 3. Gaps between mould wall and chip surface

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Table 2. Dimension of 3D SCP model [19] used in the FLUENT modelling

Item	Dimension
Silicon chips	10 mm (H) × 10 mm (W) × 0.1 mm(T)
Silicon substrate	20 mm (H) × 20 mm (W) × 0.625 mm (T)
Bump radius	100µm
Bump thickness	35 µm
Via radius	35 µm
Via pitch	800 µm

(H = height; W = width; T = thickness)

FLUENT Modelling

In the analysis, the SCPs were built and meshed according to the dimensions as presented in Table 2. The finite-volume-based software, FLUENT 6.3.26, was utilised to model the fluid flow and solve the governing equation of the EMC flow field in the encapsulation process. A total of 70,000–1,600,000 tetrahedral elements were meshed in the 3D model of the packages, as illustrated in Figure 4.

The epoxy compound, EME 6300HN [5], and air were considered as the phases in the simulation. The Castro-Macosko viscosity model and Kamal's equation were programmed to model the flow behaviour and curing kinetics of the EMC. The VOF technique was applied to track the melt front advancement in the encapsulation, in which the mould temperature (T_w) was set at 170°C with inlet pressure (p_{in}) of 1 MPa and preheat temperature of 90°C. The EMC material properties are summarised in Table 3.

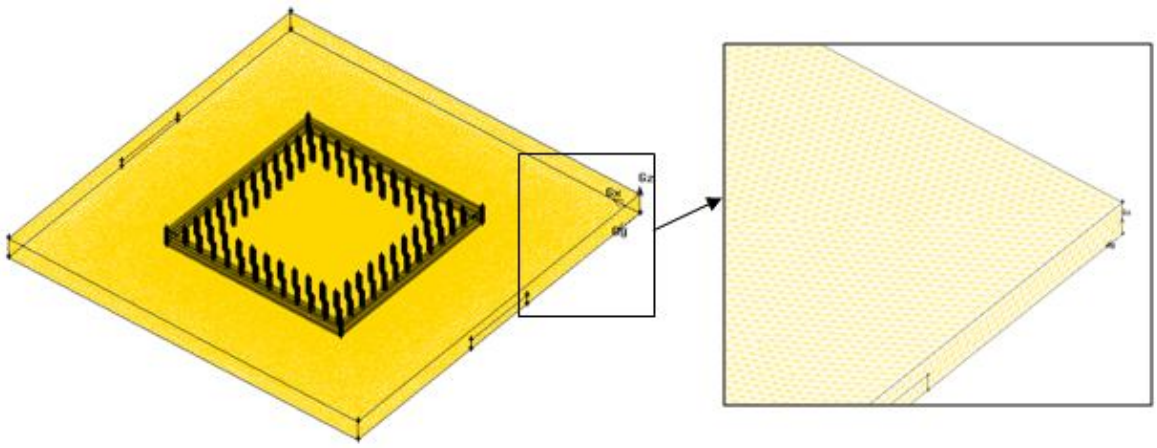

Figure 4. Meshed model for SCP (six chips)

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Table 3. EMC material properties [5] used in FLUENT simulation

Castro-Macosko model parameter		Kamal model parameter	
B (kPa.s)	3.81E-7	m_1	1.21
T_b (K)	5230	m_2	1.57
α_g	0.17	A_1 (1/s)	33.53E3
C_1	1.03	A_2 (1/s)	30.54E6
C_2	1.50	E_1 (K)	7161
		E_2 (K)	8589

The first-order upwind discretisation was utilised for both momentum and energy equations, with the SIMPLE scheme for pressure-velocity coupling. A time-dependent formula and an implicit solution were applied for the volume fraction in every time step. The values 'one' and 'zero' were assigned for the volume fractions of the EMC and air phases respectively. However, the user-defined functions were developed using C programming (Microsoft VISUAL STUDIO.NET) and incorporated into the FLUENT simulation to solve the Castro-Macosko model and Kamal's equation. An optimum time step of 0.001 sec. was applied in the simulation and 3400 time steps were taken to fill the mould cavity completely. The simulations were analysed using a computer with Intel Core i3 processor i3-540 at 3.07 GHz and 3.24 GB of RAM.

The boundary conditions of the 3D models were defined in the FLUENT analysis as illustrated in Figure 5. The boundary and initial conditions are as follows:

a) On wall : $u = v = w = 0$; $T = T_w$, $\frac{\partial p}{\partial n} = 0$

b) On centre line : $\frac{\partial u}{\partial z} = \frac{\partial v}{\partial z} = \frac{\partial w}{\partial z} = \frac{\partial T}{\partial z} = 0$

c) On melt front : $p = 0$

d) At inlet : $p = p_{in}(x, y, z)$; $T = T_{in}$

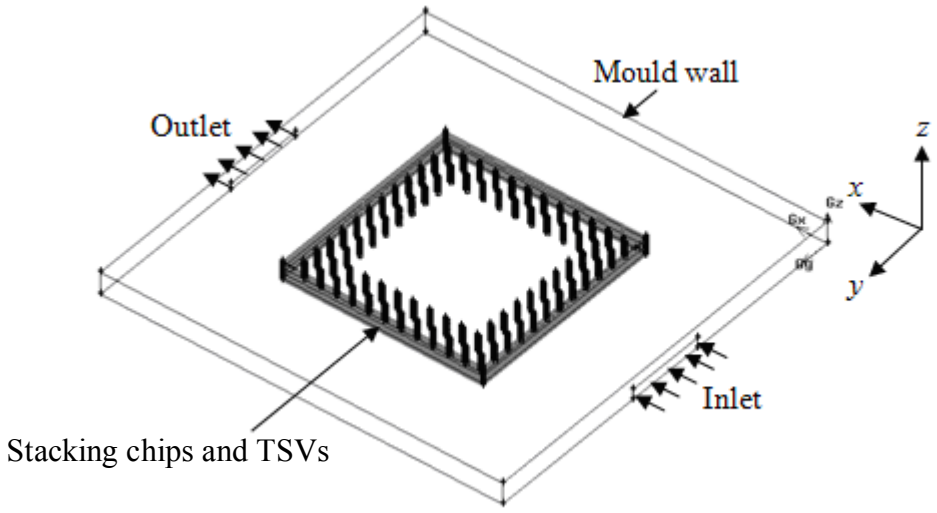

Figure 5. Boundary conditions of the IC package

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ABAQUS Modelling

The present structure analysis solves the deformable structure of the TSVs during the encapsulation process using the FEM-based software, ABAQUS. The TSV model was built based on the dimensions in Table 2 and meshed using tetrahedral elements as shown in Figure 6. The structure of the copper TSVs was designated an elastic modulus E = 113.85 GPa and a Poisson ratio v = 0.35. The mechanical properties of the silicon chip and copper are summarised in Table 4. The fixed boundary condition of the structural model was set at the bottom of the TSV.

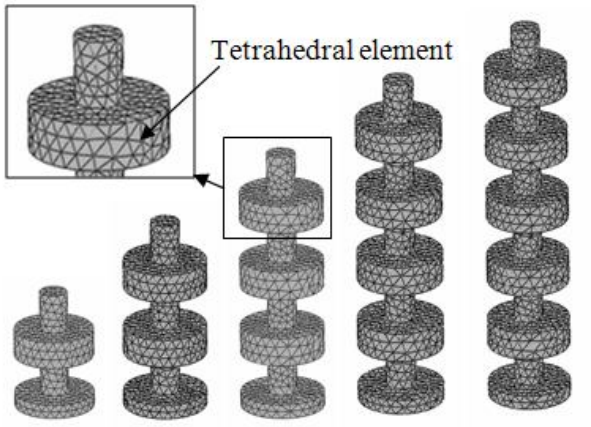

Figure 6. Meshed TSV model for structural analysis using tetrahedral elements

Table 4. Mechanical properties for the FEM analysis [16] using ABAQUS

Material	Elastic modulus, E (GPa)	Poisson ratio, ν
Copper	113.85 [32]	0.35
Silicon	125	0.28

RESULTS AND DISCUSSION

In the present study, the designed inlet-outlet heights were set for the package design as mentioned earlier. The effects of the number of stacking chips on computing time, meshing elements, flow front advancement profile, pressure distribution in the cavity, void formation, drag force, displacement, and stress of the TSVs in the encapsulation process are then discussed.

Model Validation

The predictions of the flow-front advancement for the SCP encapsulation process are impossible because of the lack of experimental data on 3D SCP with TSVs. However, the prediction of the encapsulation and injection mould modelling by the present methodology was well validated in previous studies [6, 33-34]. The prediction of flow-front advancement and viscosity variation matched well with the experimental results. Figure 7 shows a comparison of simulation and experimental results [5] for the TQFP encapsulation process. Both results showed similar filling trends during the process. From the comparison, the strength of FLUENT in handling encapsulation

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problems was proven. Thus, the predictions of 3D SCP encapsulation could be accomplished using the designed model.

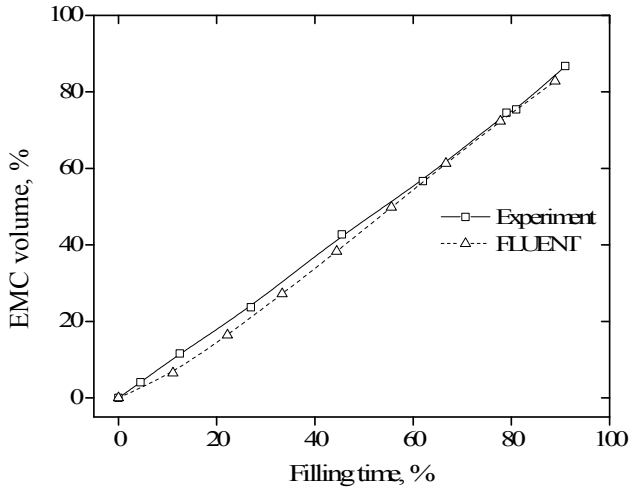

Figure 7. Comparison of simulation and experimental data on EMC volume filled versus filling time during the encapsulation process

Computing Time and Number of Meshing Elements

Generally, the computational fluid dynamics software [6, 35] is widely utilised to handle various engineering problems. The application of this software involves computing time of the simulation, which is always related to the cost in the research work. The modelling and simulation of the complicated 3D model may require more computing time and higher cost. Figure 8 shows that the number of meshing elements is directly proportional to the number of stacking chips in the cases 1–5 (Table 1). As the number of stacking chips increases, the package volume rises, increasing the number of meshing elements in the modelling process. The correlation of computing time and meshing elements is plotted in Figure 9. The computing time is directly proportional to the number of meshing elements in the simulation based on the finite volume method.

Fluid Flow Analysis

The designed inlet-outlet of the IC package was employed for packages with different numbers of stacking chips and increasing inlet and outlet heights. Figure 10 shows the filling volume of the packages versus encapsulation time. Comparison of the filling volume for different cases shows that the increase in number of stacking chips directly increases the package volume. The designed inlet-outlet enabled the volume of the filled packages to follow a similar trend. All packages were almost filled at 3.4 sec. When the inlet gate height was increased, more EMC was fed into the cavity, thus reducing the filling time. The application of the designed inlet-outlet heights (h_{in}=0.5t and h_{out}=0.25t) in the IC package maintained the encapsulation time during the process for the different cases with diverse package volumes and stacking chips at a constant inlet pressure. Furthermore, the design of a multi-inlet gate [6] and optimum inlet location [11] could effectively minimise the filling time in the encapsulation process. Therefore, the process could be controlled through the design of the inlet and outlet areas of the mould cavity.

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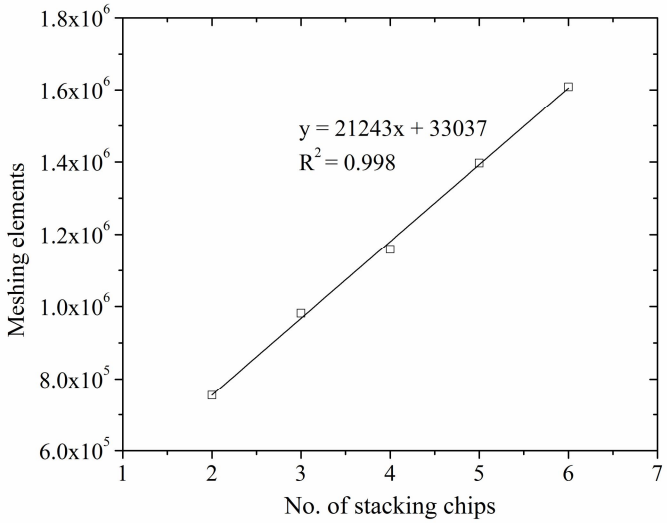

Figure 8. Number of meshing elements in cases 1-5 (No. of stacking chips = 2-6)

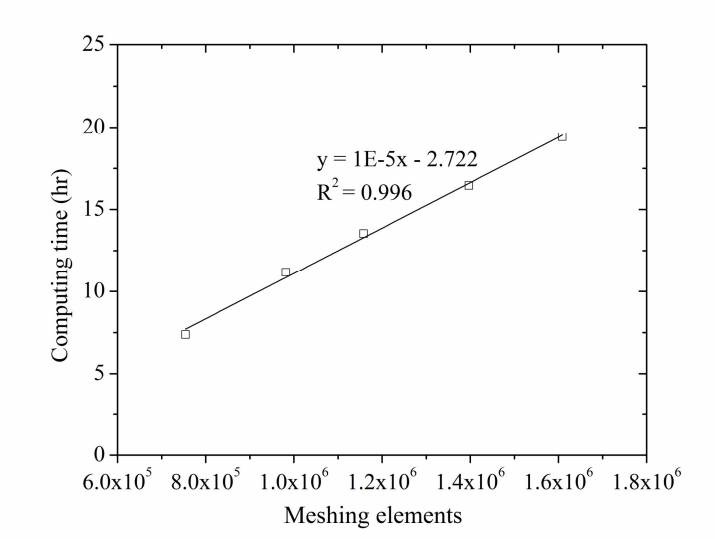

Figure 9. Computing time versus meshing elements

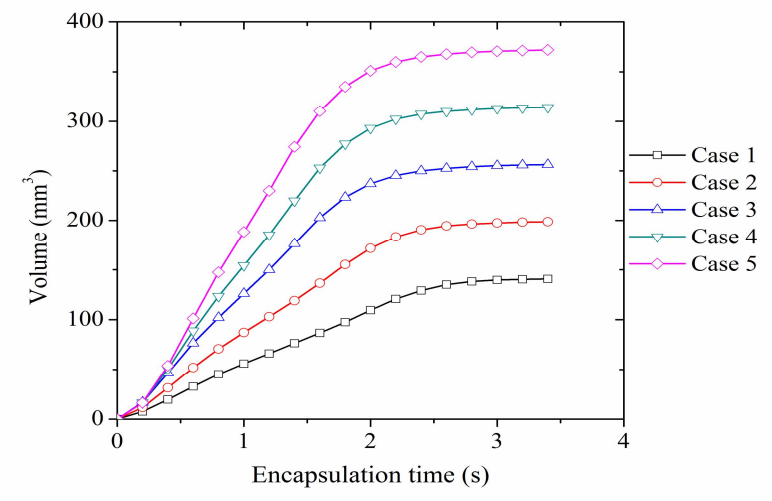

Figure 10. Volume filled during encapsulation

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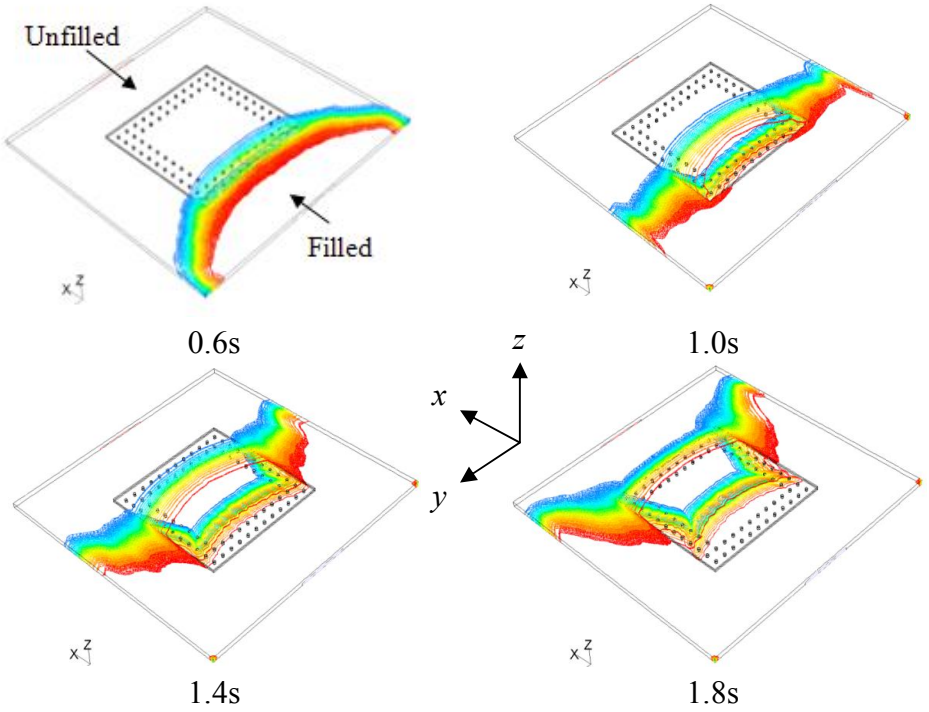
Flow-Front Advancement

Figure 11 shows the flow-front advancement of the EMC in the SCP at filling times of 0.6, 1, 1.4 and 1.8 sec. during the encapsulation process. As shown, the EMC interacts with the silicon chips and TSVs. The filled and unfilled regions are labelled at 0.6 sec. for each case. The interaction between the moulding compound and the stacking chips occurs at approximately 0.6 sec for each case. Figure 11(a) shows the non-uniform front advancement at 1.0 sec., when the compound flows through gap h_1 (between the top surface of the stacking chips and the mould wall). The flow that passes through gap h_1 is faster than that through the gap between the stacking chips and gap h_2. The small gap between the stacking chips resists the EMC flow and this phenomenon is observed at 1.4 sec. A faster flow at the free regions (no stacking chips) begins at 1.4 sec. until 1.8 sec. The compound completely fills gap h_1 at 1.8 sec. However, unfilled regions still exist in the gap between the stacking chips and gap h_2.

The increase in inlet and outlet areas at a constant inlet pressure significantly influences the flow behaviour (Figures 11(b-e)). More EMC is fed into the cavity with a larger inlet area, as clearly shown at 0.6 sec. The free region in the package increases when the number of stacking chips increases, enabling the EMC to flow more freely and faster than around the stacking chips. This situation is observed in cases 2–5 at filling times of 1.0 and 1.4 sec. A high possibility of void formation around the gap between the stacking chips is identified when the compound totally fills the free regions, as illustrated in Figures 11(b-e) at the filling time of 1.8 sec.



(a) 2 stacking chips (Case 1)

Figure 11. Flow-front advancement of EMC in the packages. Colours in Figure represent volume fractions ($0<F<1$) of cells (as mentioned in governing equations), which illustrate EMC flow front advancement during the encapsulation process.

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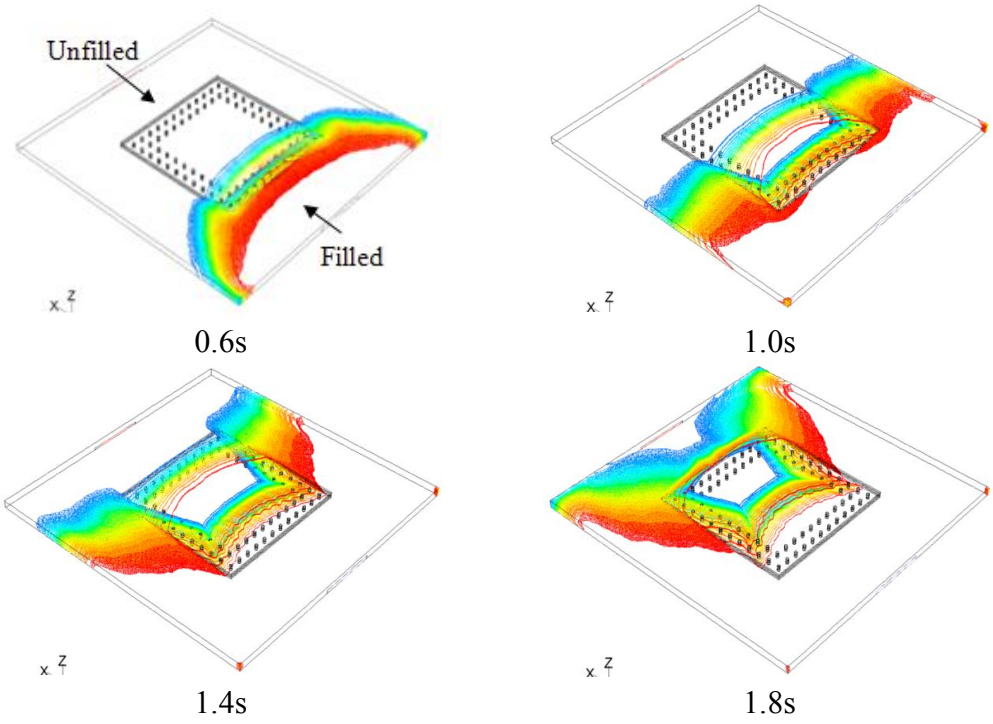
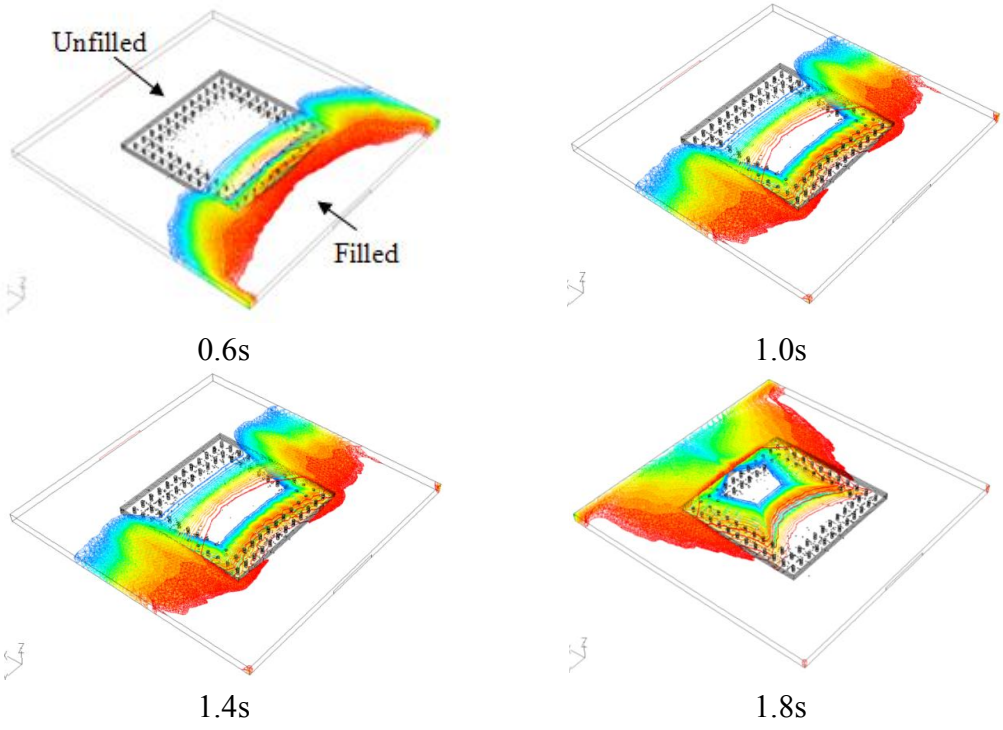


(b) 3 stacking chips (Case 2)



(c) 4 stacking chips (Case 3)

Figure 11 (Cont.)

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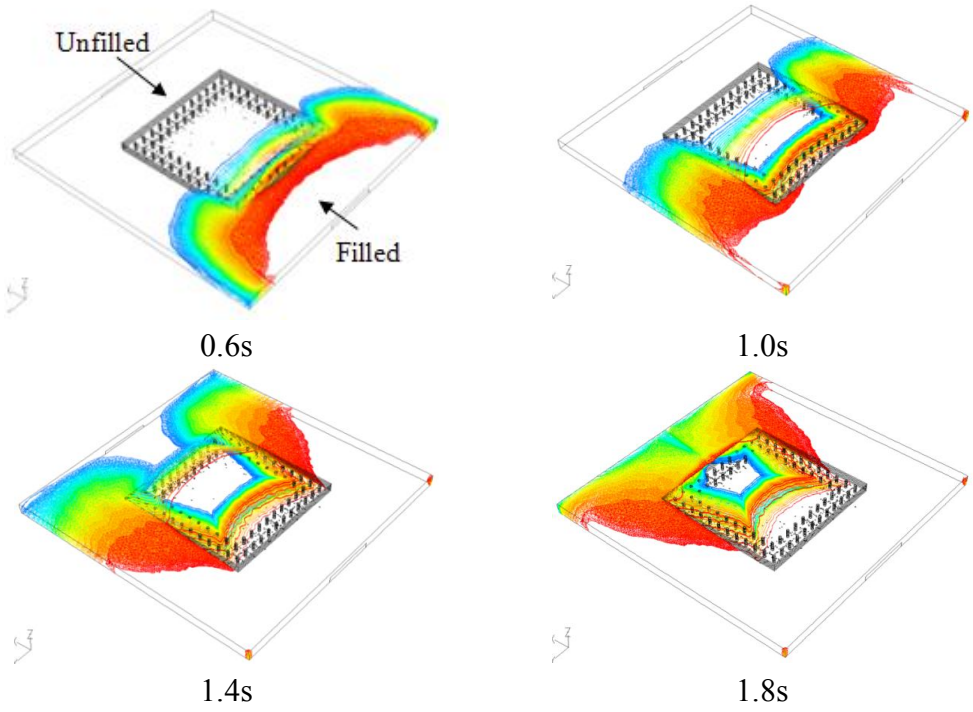
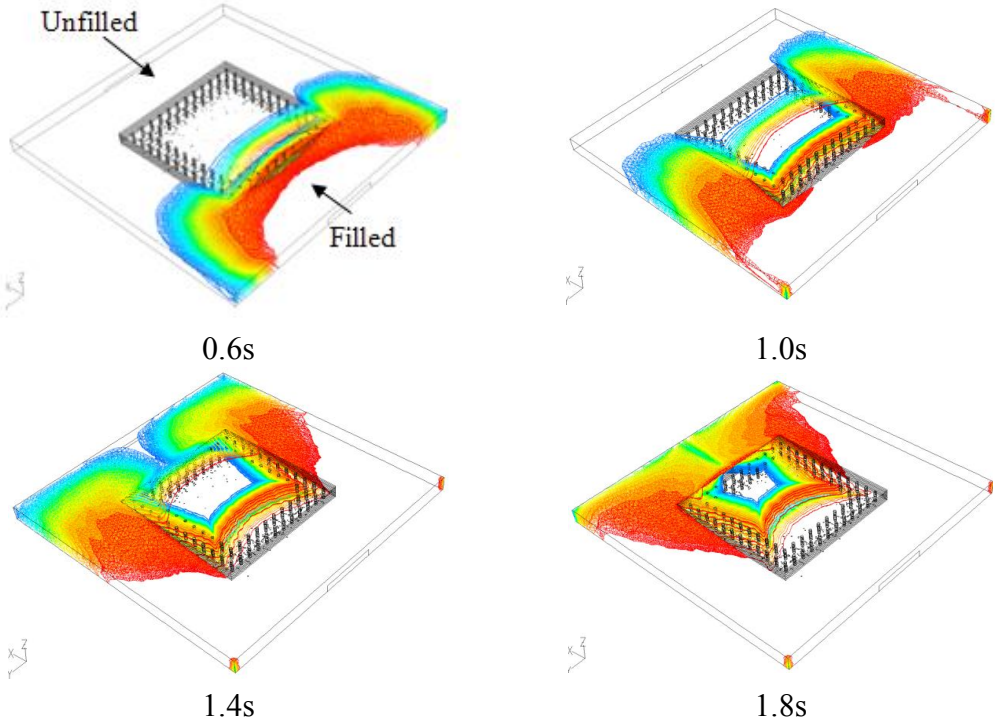


(d) 5 stacking chips (Case 4)



(e) 6 stacking chips (Case 5)

Figure 11 (Cont.)

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Pressure Distribution

The inlet gate design significantly affects the flow front, filled volume and filling time at constant inlet pressure. Therefore, the pressure in the cavity during encapsulation was measured at different positions, as illustrated in Figure 12. The pressure points, P1 to P5, are positioned at the cavity near the stacking chips. P1 and P5 are located at the free regions, whereas P2 and P4 are positioned around the corner of the stacking chips. P3 is positioned between P2 and P4.

Figure 13 shows the measured pressure at P1 to P5 at 2.6 sec. of the encapsulation process before the plunger stops. The pressure variations for all cases show similar trends. The pressure in the cavity is due to the presence of the EMC. As shown in Figure 13, the increase in the inlet height and number of stacking chips raises the pressure in the cavity. This increase may be attributed to the volume of EMC that is fed into the cavity. As the gate height increases, more EMC fills the cavity, thus increasing the cavity pressure. A similar phenomenon was found in the TQFP encapsulation process [6]; the increase in the number of inlet gates raised the cavity pressure. The pressure at P3, which is located in front of the inlet gate, is highest because of a continuous fluid flow from the inlet gate and the obstruction created by the stacking chips. The pressure of the fluid flow at P1 and P5 is lowest because of the absence of stacking chips. The correlations between the inlet gate height (h_{inlet}) and pressure at P1, P2 and P3 are presented in Figure 14. Based on the Figure, the cavity pressure is directly proportional to the inlet gate height.

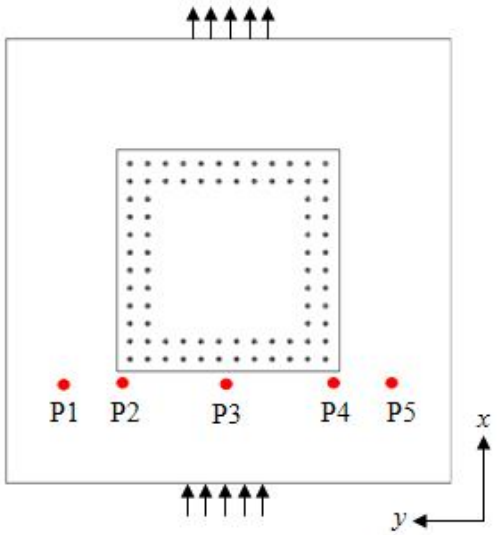

Figure 12. Points P1 to P5 where pressure was measured near the stacking chips

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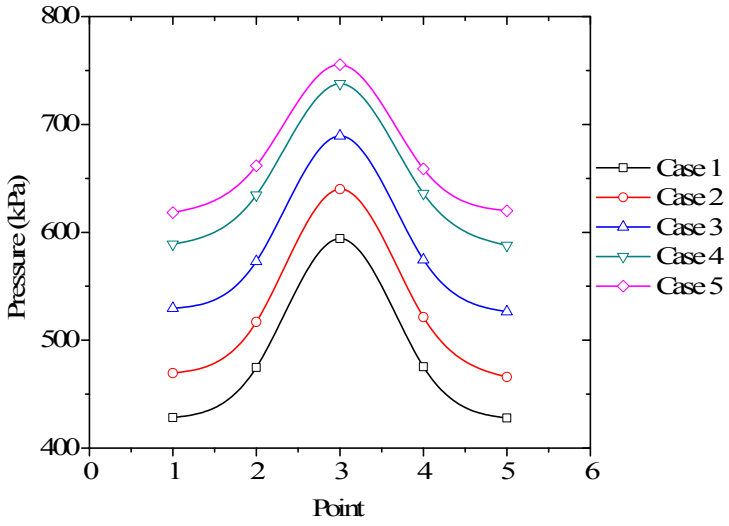

Figure 13. Pressure at points P1–P5 measured at 2.6 sec. of encapsulation for different cases

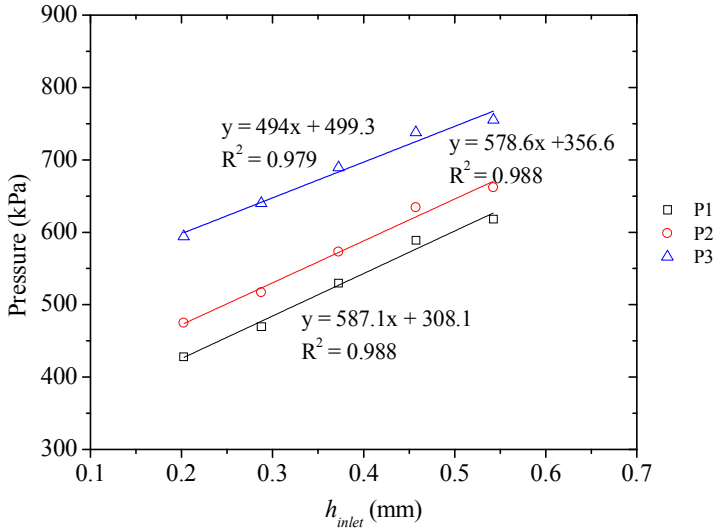

Figure 14. Pressure versus h_{inlet} at P1, P2 and P3

Void Formation

The void formation in the IC package causes the diminution of the package reliability. The number of stacking chips crucially influences the void formation. The voids were formed at the gaps between the stacking chips during encapsulation [31]. To reduce the void in IC packaging, the present study considers the inlet gate height (h_{inlet}). Figure 15 shows the percentage of void formation in the packages for different h_{inlet} values obtained from the current study. As mentioned earlier, h_{inlet} increases as the number of stacking chips increases. The void formation is reduced when h_{inlet} increases as more EMC fills the cavity. The use of a multi-inlet or optimised gate minimises the void formation in the packages [6, 11]. Thus, the use of the designed inlet-outlet heights ($h_{inlet} = 0.5t$ and $h_{outlet} = 0.25t$) is important for the present stacking-chip IC package design in reducing the void formation.

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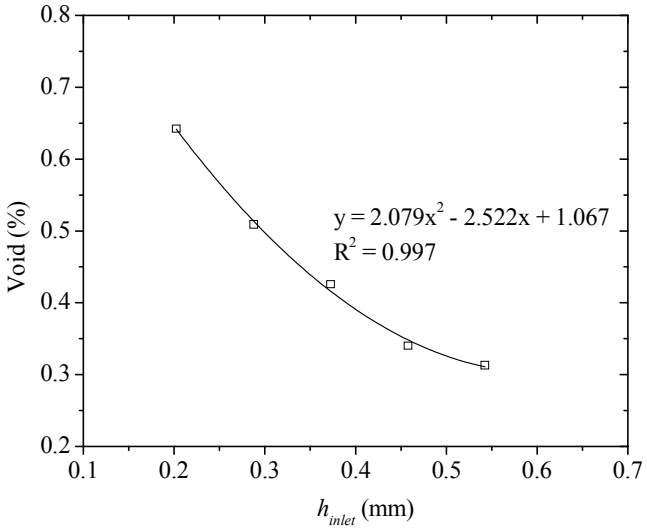

Figure 15. Percentage of void formation in the packages

The positions of the void formation in the packages are presented in Figure 16. The voids are observed at the bottom gap (h_2) for all cases because of the smaller gap between the mould and chip surface. Figure 16 shows the shape and position of the voids, which are concentrated at the edge of the chips nearer to the outlet. Almost identical locations were identified in all cases with only small difference in void shape. The void formation phenomenon was investigated and the flow of the EMC is illustrated in Figure 17. The faster flow in the free regions and gap h_1 completely covers the stacking chips while the air is trapped in the space between the chips and the bottom mould wall, making the EMC unable to flow through the unfilled region. Thus, a void is formed in the package.

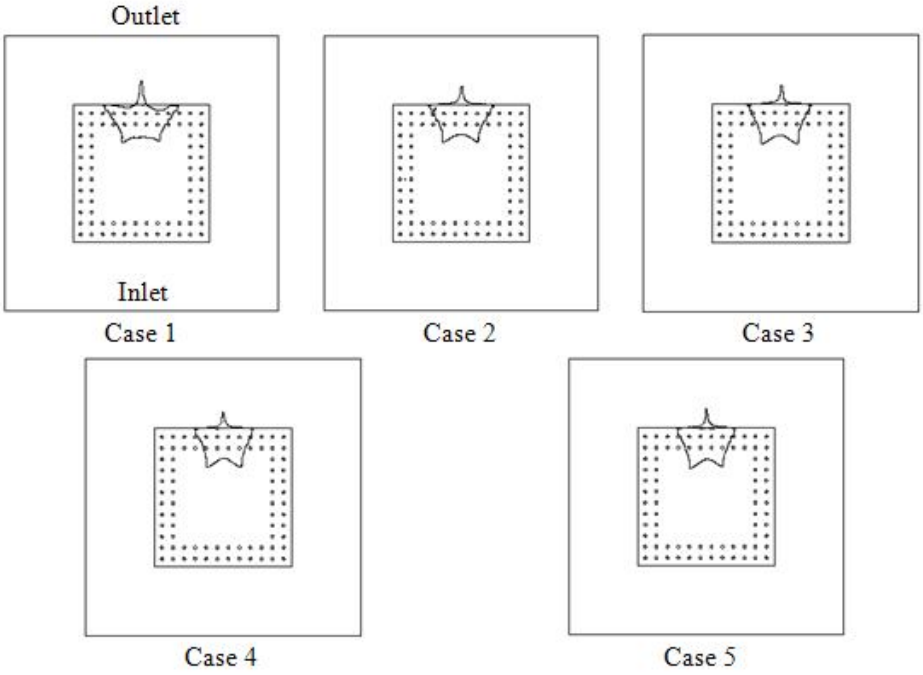

Figure 16. Location of voids from the bottom view

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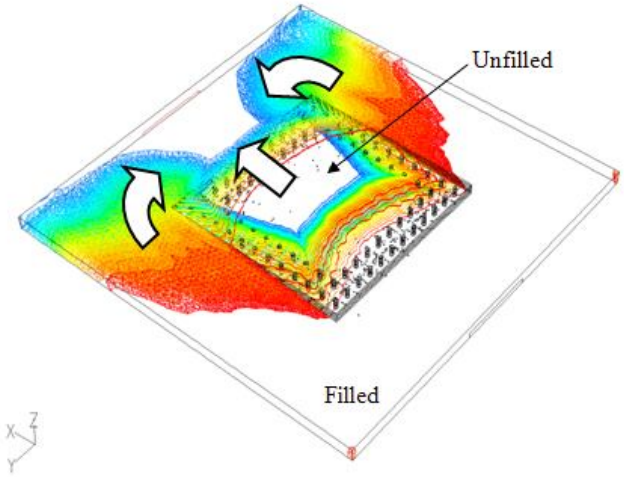

Figure 17. Phenomenon of void formation

Drag Force on Stacking Chips and TSVs

Viscous fluid flow induces drag force to the silicon chips and TSVs during the encapsulation process. The increase in h_{inlet} increases the drag force of the EMC, as shown in Figure 18. The drag force is directly proportional to h_{inlet}. The force acting on the stacking chips and TSVs can cause undesirable displacement and the tendency of the TSVs and chips to fracture in subsequent processes.

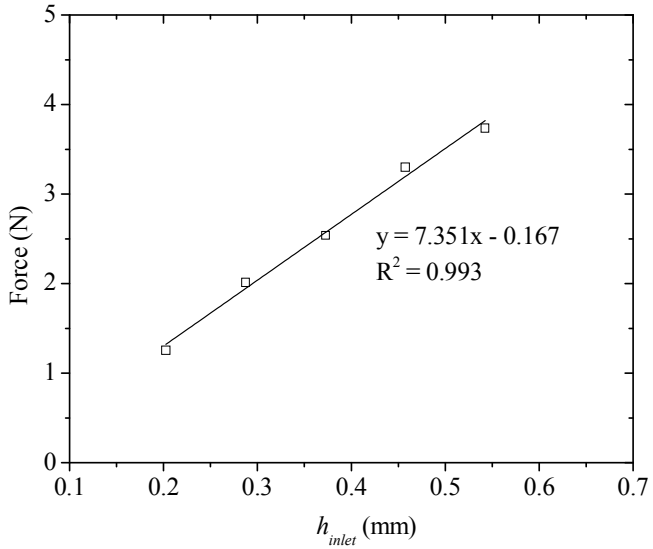

Figure 18. Drag force acting on the stacking chips and TSVs at time 2.6 sec.

Structural Analysis

The drag force induced by the viscous fluid flow was considered in the structural analysis. The TSV structure was modelled and analysed using the finite-element-based software ABAQUS 6.9. Figure 19 shows a schematic diagram of the fluid flow through the silicon chip and TSVs. In the present study, the simplification of the copper TSV integration is considered in the analysis and the force acting on the structure is assumed as uniform in the *x*-direction corresponding to the

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direction of the EMC flow. From the analysis, the displacement of the TSVs in the *x*-direction as a function of h_{inlet} is plotted in Figure 20; an increase in the stacking chips causes a higher displacement and consequent reduction in their rigidity. Figure 21 shows the displacement profile of the TSV structure with different numbers of stacking chips. The displacement occurs mainly at the top of the structure. This situation may be attributed to the fixed boundary condition at the bottom of the TSVs and the fluid-structure interaction that subjects the TSVs to the drag force of the fluid flow. The drag force induced by the EMC fluid deforms the TSV structure and the von Mises stress [21-23] is used to evaluate the stress on the structure. The von Mises stress of the TSV structure for each case is presented in Figure 22, which illustrates the von Mises stress distribution on the TSVs. The stress distribution shows a quadratic relationship with the increasing number of stacking chips. The stress is concentrated at the first layer of the TSV, which is near the fixed boundary as illustrated in Figure 23. A proper package design and control of the encapsulation process is important in minimising the structure deformation and stress of TSVs to maintain package reliability.

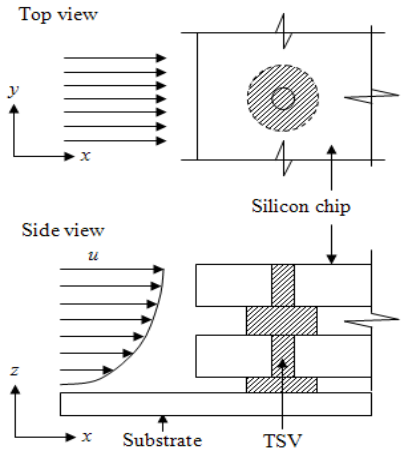

Figure 19. Fluid flow through silicon chips and TSVs

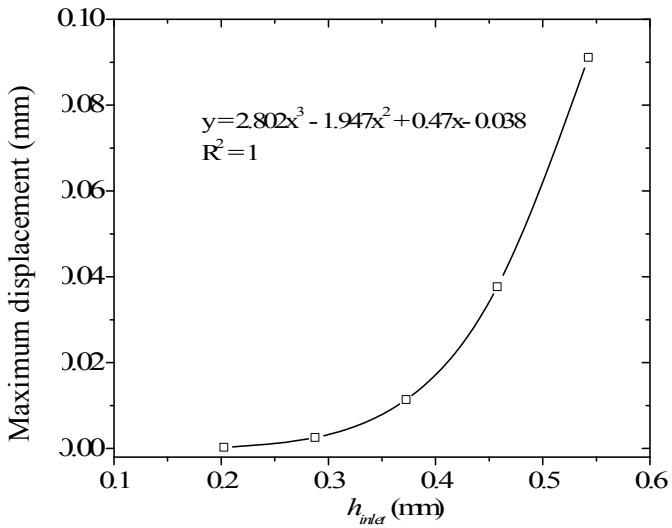

Figure 20. Maximum displacement of TSVs in x-direction

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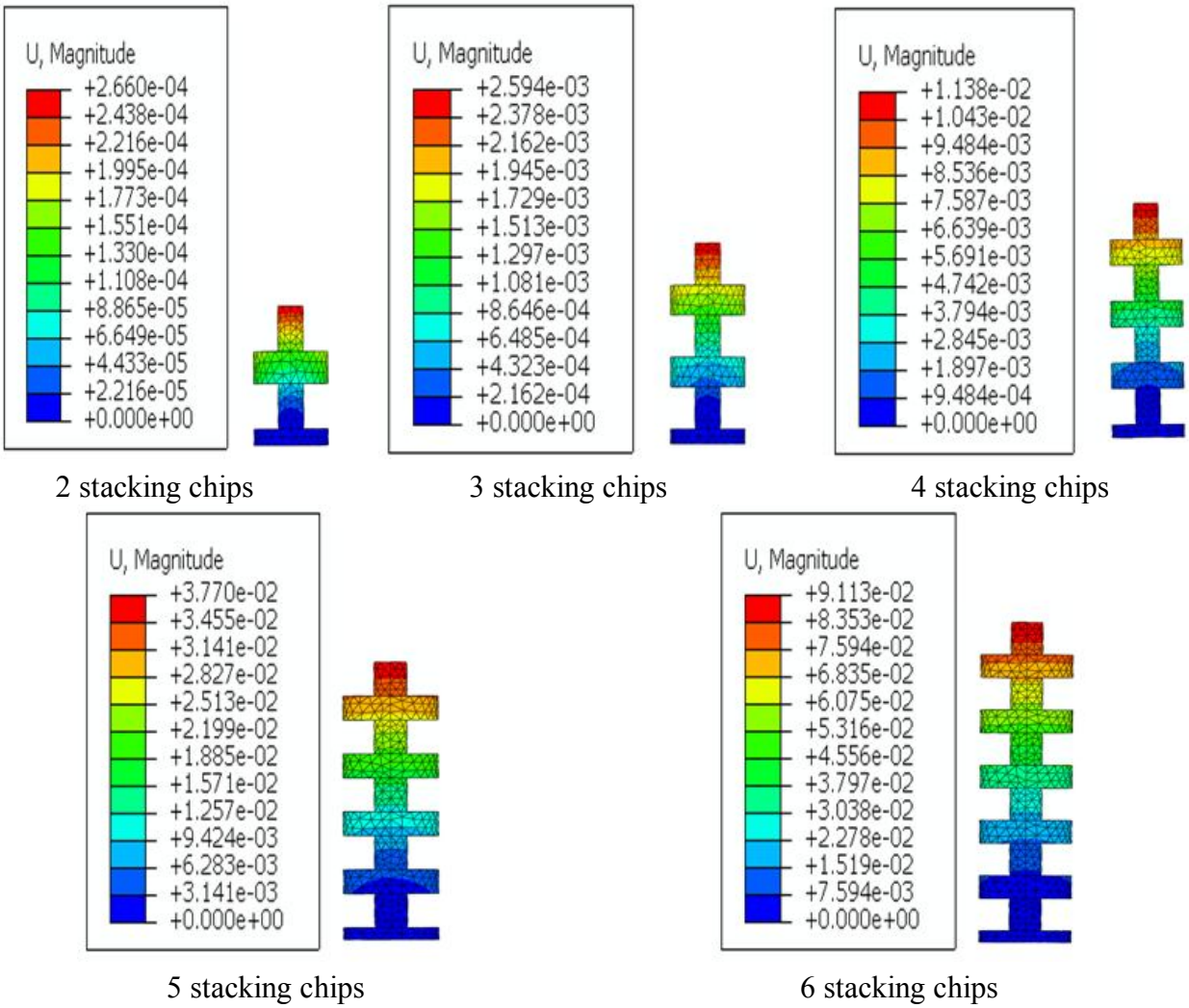

Figure 21. Magnitude of displacement (U, mm) profile of TSVs with different numbers of stacking chips

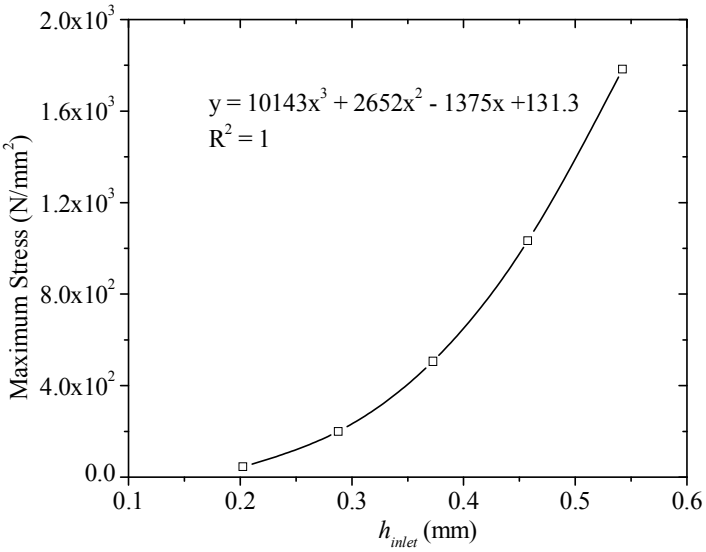

Figure 22. Maximum von Mises stress on TSV

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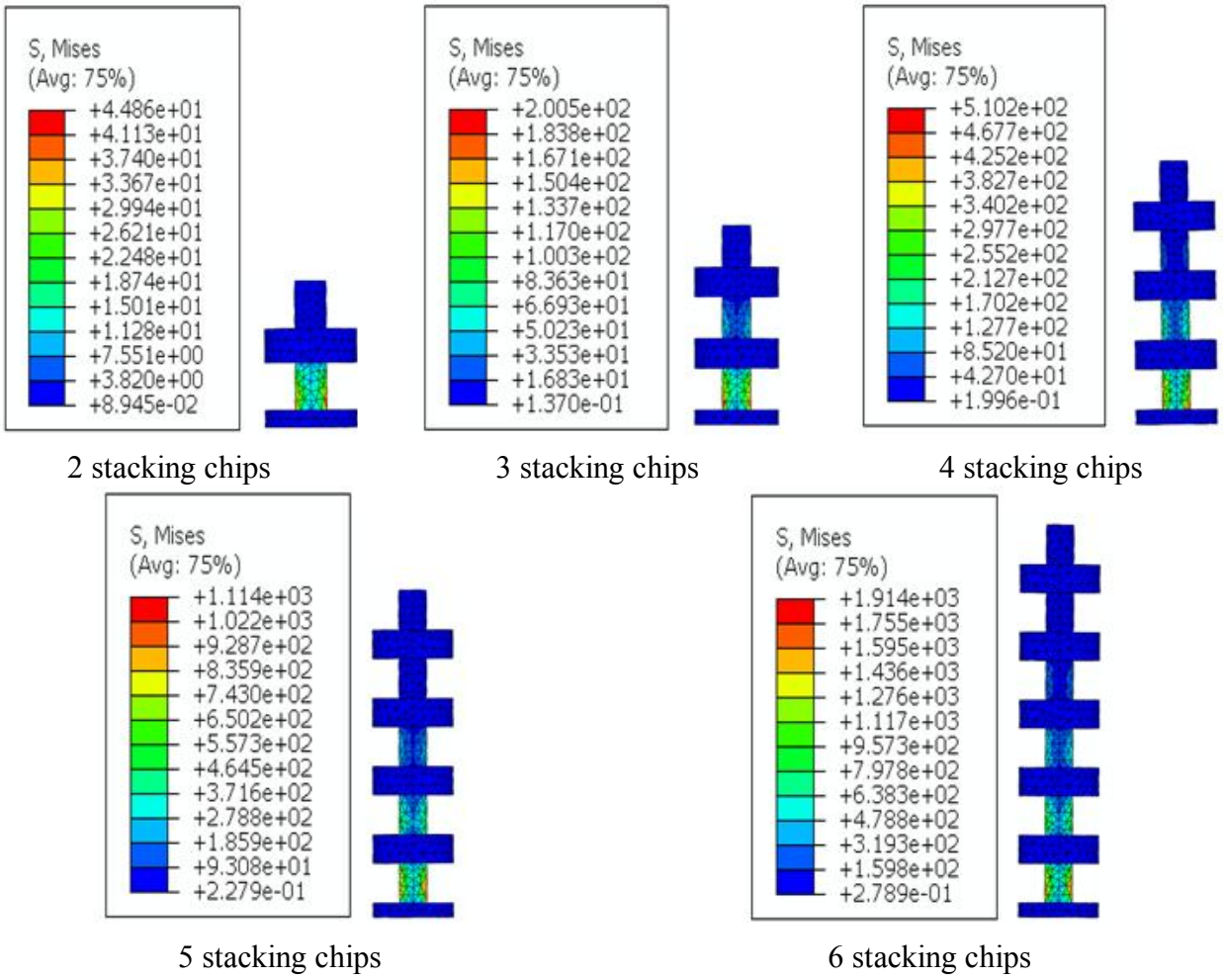

Figure 23. Von Mises stress (N/mm^2) profile of TSVs with different numbers of stacking chips

CONCLUSIONS

The application of the designed inlet-outlet heights in the encapsulation of 3D SCP has been investigated using FLUENT and ABAQUS softwares. The computational time indicated a direct correlation to the number of meshing elements in the finite volume method modelling. Increasing the inlet gate height in the IC packaging maintained the encapsulation time and reduced the percentage of void formation by slightly influencing the void shape in the package as the number of stacking chips increased. The void location was identified to be nearly identical in all cases at gap h_2 close to the outlet gate. It was found that the pressure and drag force induced by the EMC, which caused a larger displacement at the top part of the TSVs was directly proportional to the inlet gate height. However, the stress was concentrated at the lower part of the TSVs.

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