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Full Paper

Voltage controlled resistor using quasi-floating-gate MOSFETs

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Abstract: A voltage controlled resistor (VCR) using quasi-floating-gate MOSFETs (QFGMOS) suitable for low voltage applications is presented. The performance of the VCR implemented with QFGMOS is compared with its floating-gate MOSFET (FGMOS) version. It was found that QFGMOS offers better performance than FGMOS in terms of frequency response, offsets and chip area. The VCR using QFGMOS offers high bandwidth and low power dissipation and yields high value of resistance as compared to its FGMOS counterpart. The workability of the presented circuits was tested by PSpice simulations using level 3 parameters of 0.5μm CMOS technology with supply voltage of ± 0.75V. The simulations results were found to be in accordance with the theoretical predictions.

Keywords: voltage controlled resistor, floating- gate MOSFET, quasi-floating-gate MOSFET

INTRODUCTION

Implementation of active resistors in integrated circuits is desired for minimal chip area and high accuracy. An MOS transistor operating below saturation region can implement a voltage controlled resistor (VCR) but with a limited range. These VCRs are useful in the design of tunable analog circuits such as voltage controlled oscillators, automatic gain controllers, voltage controlled filters, current-mode dividers and trans-resistance amplifiers [1-4]. The design of analog circuits operating with low voltage and dissipating low power is significant for mixed-mode implementation of systems on chip which comprises both digital and analog components. For scaled-down analog circuits, the threshold voltage of the MOS transistor poses a limitation for low voltage design and it is not expected to be too low in sub-micron technologies [5, 6]. A floating-gate MOSFET (FGMOS) is a possible solution to this problem, which offers tunability of threshold voltage with a bias voltage without the need of actually lowering the threshold voltage. However, FGMOS has certain limitations like isolated floating-gate, which may accumulate static charge, give low frequency response and need large chip area [7, 8]. These limitations can be further overcome by quasi-floating-gate MOSFET (QFGMOS). In QFGMOS, the gate is not floating like in FGMOS but is weakly connected to one of the supply rails through a high

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value resistor. Besides, lowering the supply voltage requirements, QFGMOS offers better frequency response and needs less chip area [9]. It is therefore expected that the QFGMOS based VCR would exhibit better characteristics as compared to its FGMOS version.

In this paper, we have implemented a QFGMOS-based VCR and compared its performance with its FGMOS version. It is observed through both the mathematical equations and PSpice simulations that for a given value of control voltage (V_C = 0.3V) QFGMOS-based VCR exhibits a higher value of resistance (R_{eq} =1.48 kΩ) and larger bandwidth (3.61 GHz), whereas FGMOS-based VCR simulates a resistance value of 1.30 kΩ with a bandwidth of 490 MHz.

METHODS

Quasi-Floating-Gate Transistor

The equivalent circuit of the n-input N-type QFGMOS is shown in Figure 1. The input terminals are capacitively coupled to the quasi-floating gate (QFG) and its gate voltage (V_{QFG}) is set to V_{DD} through a pull-up resistor which can be implemented by using the large leakage resistance of the reverse biased p-n junction of a PMOS transistor operating in cut-off region.

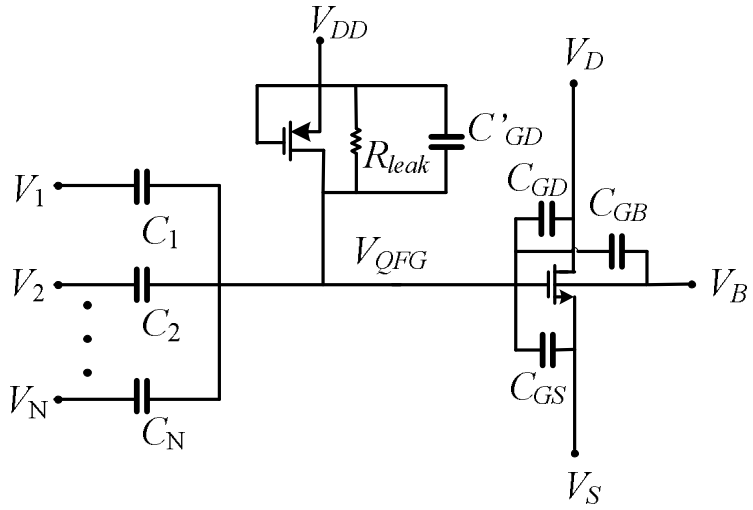

Figure 1. Equivalent circuit of QFGMOS

The quasi-floating gate voltage (V_{QFG}) in Figure 1 can be expressed as

$$V_{QFG} = V_{in} \frac{sR_{leak}C_{Total}}{1 + sR_{leak}C_{Total}} \tag{1}$$

where

$$C_{Total} = \sum_{i=1}^{N} C_i + C_{GS} + C_{GD} + C_{GB} + C'_{GD} \tag{2}$$

and

$$V_{in} = \frac{1}{C_{Total}} \left(\sum_{i=1}^{N} C_i V_i + C_{GS} V_S + C_{GD} V_D + C_{GB} V_B \right) \tag{3}$$

On substituting Equation (3) in Equation (1), V_{QFG} becomes

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$$V_{QFG} = \frac{1}{C_{Total}}\left(\sum_{i=1}^{N} C_i V_i + C_{GS} V_S + C_{GD} V_D + C_{GB} V_B\right)\left(\frac{sR_{leak} C_{Total}}{1 + sR_{leak} C_{Total}}\right) \quad (4)$$

We observe from Equation (4) that input signals encounter a high-pass filter with a cut-off frequency of $(2\pi R_{leak} C_{Total})^{-1}$, which is very low due to large value of R_{leak}. Therefore, even for very low frequencies, Equation (4) becomes a weighted average of the AC input voltages determined by capacitance ratios plus some parasitic terms. The pull-up resistor R_{leak} sets a DC voltage equal to V_{DD} on the quasi-floating gate upon which an AC voltage given in Equation (4) is superimposed. Hence, the gate voltage can become larger than V_{DD}. Similarly for P-type QFGMOS, a pull-down resistor sets the DC gate voltage to V_{SS}, which is implemented by a reverse biased p-n junction of an NMOS transistor in the cut-off region [10-18].

Voltage Controlled Resistor

The circuit of a simple MOS-based VCR is shown in Figure 2 where MOSFETs M1 and M2 are biased in the triode region and M2 acts as resistor whose resistance can be controlled by its gate voltage (V_C). The N-type current mirror formed by M3-M4 and P-type current mirror formed by M5-M6 ensure the same drain current in both M1 and M2. The transistors M1 and M2 are assumed to be perfectly matched transistors with the same drain currents I_1 and I_2 in the absence of input current (I_{in}) and M1 is biased in the ohmic region. This arrangement makes M2 operate in the ohmic region whose conductivity can be further varied by I_{in}. Thus, M2 acts as a variable resistor whose resistance value is controlled by V_C [19].

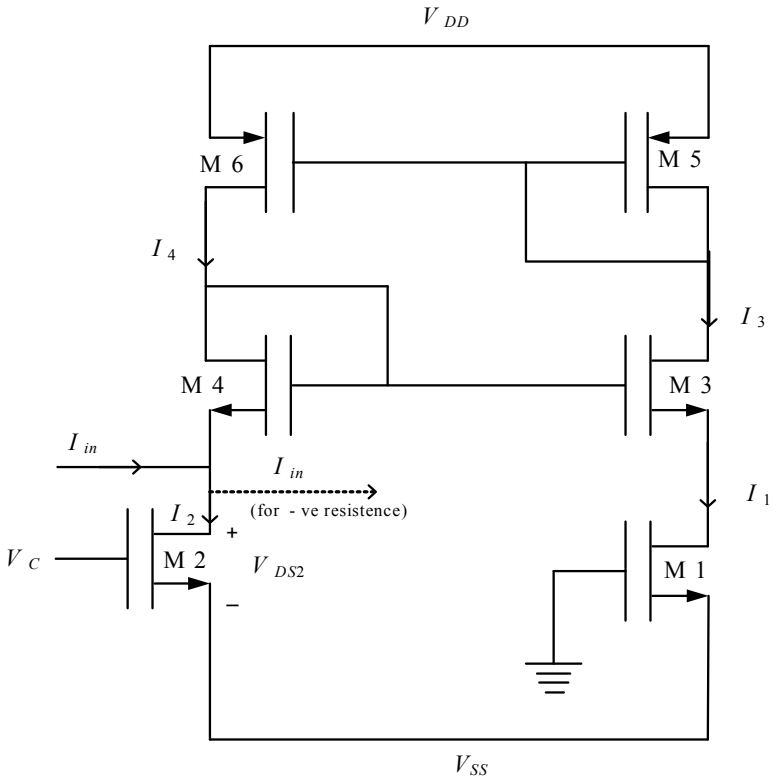

Figure 2. MOS-based VCR

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The equivalent resistance of the MOS-based VCR [3] is given by:

$$R_{eq} = \frac{V_{DS2}}{I_{in}} = \frac{1}{K_n V_C} \tag{5}$$

To ascertain the workability of the circuit shown in Figure 2, PSpice simulation was used by selecting *W/L* as 10μm/1μm for M1 and M2, 50μm/1μm for M3 and M4, 20μm/0.5μm for M5 and 40μm/1μm for M6 with a supply voltage of ± 0.75V. The simulated resistance (R_{eq}) varied with control voltage (V_C) in accordance with Equation (5) as shown in Figure 3 where the resistance varies from 2 kΩ to 1.11 kΩ as control voltage varies from 0.3 V to 0.75 V.

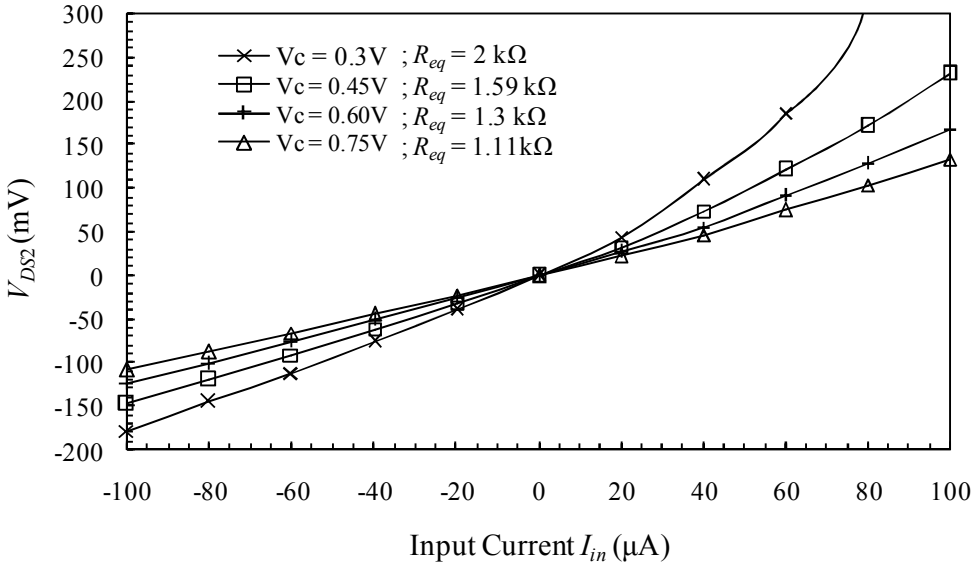

Figure 3. Resistance simulation using MOS-based VCR

QFGMOS-based Voltage Controlled Resistor

The QFGMOS-based VCR is shown in Figure 4. It differs from the FGMOS-based VCR presented [2] in that the gates of FGMOS are connected to a biased voltage through a large value capacitor ($C_2 >> C_1$) whereas the gates of QFGMOS are connected to the supply rails through reverse biased MOSFETs M8-M11.

The drain currents of M1 and M2, biased in the ohmic region are given by:

$$I_1 = K_n \left[\left\{ \left(\frac{C_1}{C_{Total}}(-V_{SS}) + \frac{C'_{GD}}{C_{Total}} V_{DD} - \frac{C_{GS}}{C_{Total}} V_{SS} \right) - V_{Tn1} \right\} - \frac{V_{DS1}}{2} \right] V_{DS1} \tag{6}$$

where

$$K_n = \frac{\mu_0 C_{OX} W}{L}$$

and

$$I_2 = I_{in} + I_4 = K_n \left[\left\{ \left(\frac{C_1}{C_{Total}}(V_C - V_{SS}) + \frac{C'_{GD}}{C_{Total}} V_{DD} - \frac{C_{GS}}{C_{Total}} V_{SS} \right) - V_{Tn2} \right\} - \frac{V_{DS2}}{2} \right] V_{DS2} \tag{7}$$

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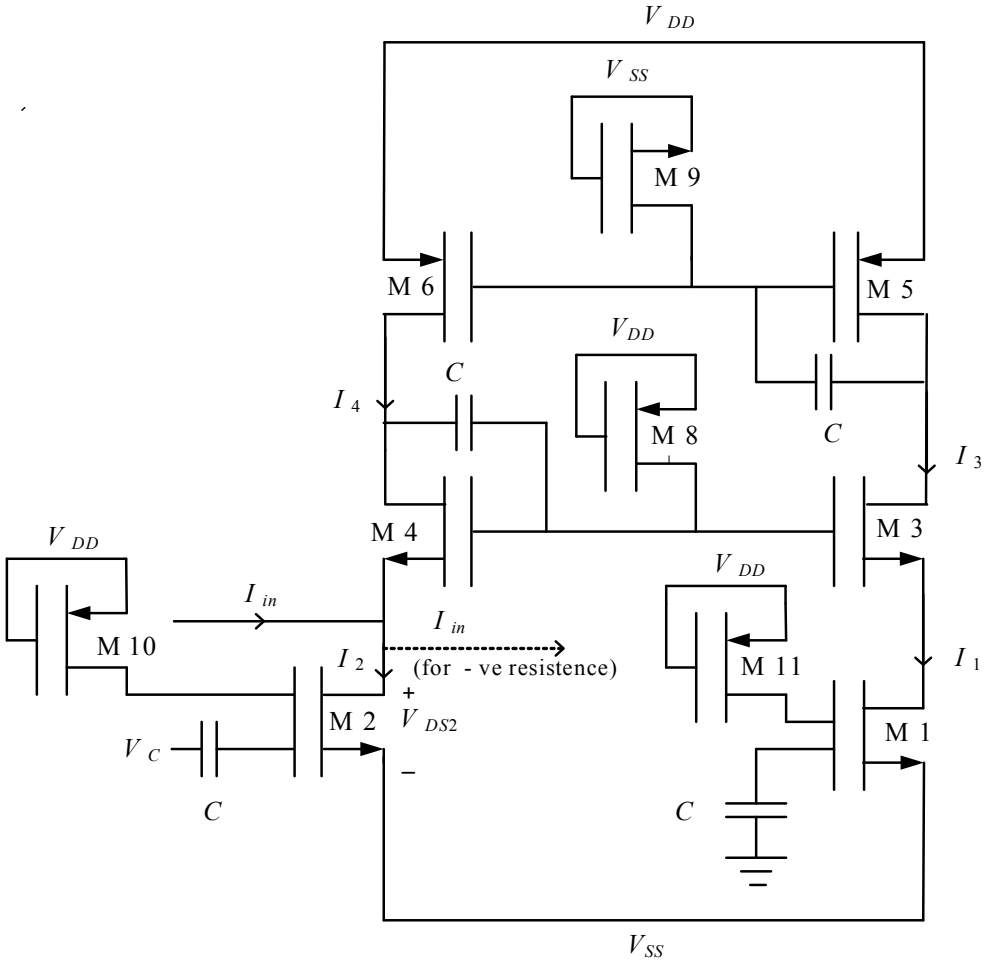

Figure 4. QFGMOS-based VCR

The current mirror arrangement of transistors M5 and M6 generates a current I_3 such that $I_3 = I_4 = I_1$. Since transistors M3 and M4 are assumed to be perfectly matched and are biased in saturation region, their drain currents are given by:

$$I_3 = \frac{K_n}{2}\left(V_{GS3} - V_{Tn3}\right)^2 \tag{8}$$

$$I_4 = \frac{K_n}{2}\left(V_{GS4} - V_{Tn4}\right)^2 \tag{9}$$

which gives

$$I_{in} = K_n\left(K_1 V_{DD} + K_2 V_C\right)V_{DS2} \tag{10}$$

From Equation (10), the equivalent resistance (R_{eq}) is given by:

$$R_{eq} = \frac{V_{DS2}}{I_{in}} = \frac{1}{K_n\left(K_1 V_{DD} + K_2 V_C\right)} \tag{11}$$

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where $K_1 = \frac{C'_{GD}}{C_{Total}} \& K_2 = \frac{C_1}{C_{Total}}$ (12)

Equation (11) reveals that the circuit in Figure 4 implements a VCR whose resistance value depends on the control voltage (V_C). The corresponding equation for R_{eq} using FGMOS [2] is given by:

$$R_{eq} = \frac{1}{K_n\left(K_1 V_b + K_2 V_C\right)} \quad (13)$$

where K_2 is the same as in Equation (11) for VCR using QFGMOS and $K_1 = \frac{C_2}{C_{Total}}$. Since $C_2 >> C'_{GD}$, the resistance value for QFGMOS-based VCR will be larger than FGMOS-based VCR at a given value of control voltage. It also results in a better frequency response of QFGMOS- based VCR than its FGMOS counterpart [8, 9].

RESULTS AND DISCUSSION

The circuit of Figure 4 was simulated using PSpice level 3 parameters with supply voltage of ± 0.75V and by selecting *W/L* of 10µm/1µm for M1 and M2, 50µm/1µm for M3 and M4, 20µm/0.5µm for M5, 40µm/1µm for M6 and 50µm/0.5µm for M8-M11. The variation of resistance with different control voltages is shown in Figure 5. It is observed that the value of the simulated resistance varies inversely with the control voltage as shown by Equation (11).

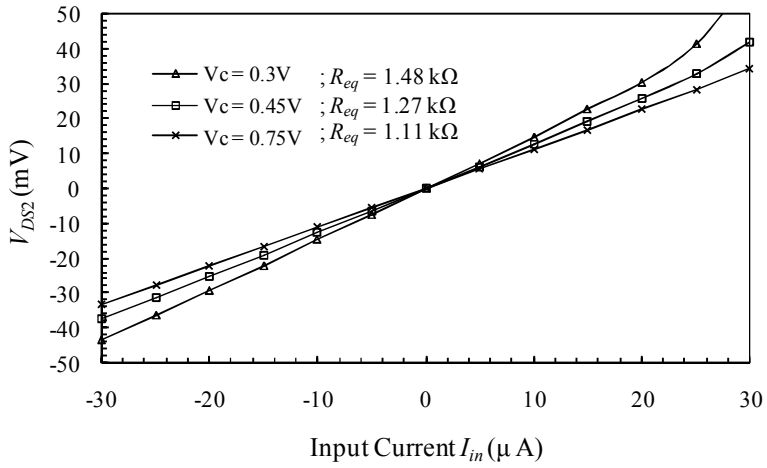

Figure 5. Resistance simulation with QFGMOS VCR

The circuit of VCR was also implemented using FGMOS and its performance compared with its QFGMOS counterpart. The performance of QFGMOS-based VCR was found to be better than that of its FGMOS version due to the inherent advantages of QFGMOS over FGMOS. The values of the equivalent resistance realised using QFGMOS vis-a-vis FGMOS for different values of V_C are given in Table 1.

It can be seen that R_{eq} decreases from 1.48 kΩ to 1.11 kΩ for QFGMOS-based VCR and from 1.3 kΩ to 1.11 kΩ for FGMOS-based VCR with the increase in V_C from 0.3 V to 0.75 V. A large value of the resistance of the order of kΩs or more can be obtained for smaller dimensions of transistors, which may lead to non-linearity.

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Table 1. Variation of R_{eq} with V_C

V_C (V)	R_{eq} with QFGMOS (kΩ)	R_{eq} with FGMOS (kΩ)
0.3	1.48	1.30
0.45	1.27	1.23
0.6	1.19	1.17
0.75	1.11	1.11

It was also found that for control voltage (V_C) of the order of supply voltage, both QFGMOS and FGMOS topology of VCR yield the same value of resistance. This can be attributed to the fact that Equations (11) and (13) approximately become identical and resemble Equation (5). when V_C approaches positive supply voltage. The frequency response of QFGMOS-based VCR at different control voltages is shown in Figure 6. It can be observed that as control voltage increases from 0.3V to 0.75V, the bandwidth of QFGMOS-based VCR increases from 3.61 GHz to 4.9 GHz with the corresponding decrease in the value of simulated resistance. The same trend has also been observed in FGMOS-based VCR [2]. When control voltage in FGMOS-based VCR increases from 0.3V to 0.75V, the bandwidth increases from 490 MHz to 576 MHz and the corresponding value of simulated resistance decreases from 1.30 kΩ to 1.11 kΩ. This is due to the fact that with an increase in control voltage, the drain current of the transistors increases, which results in higher bandwidth and lower resistance.

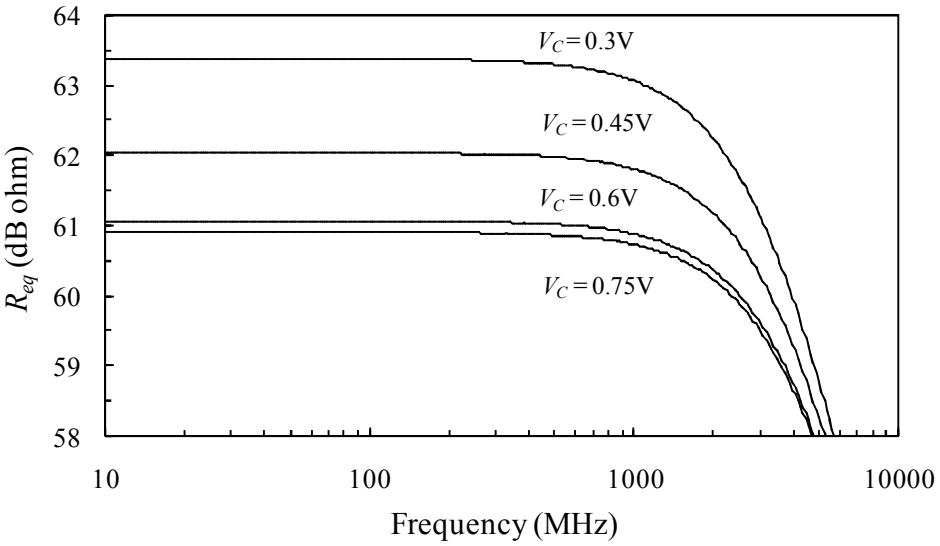

Figure 6. Frequency response of QFGMOS-based VCR

The comparative resistance simulation characteristics of VCR based on FGMOS and QFGMOS are shown in Figure 7. For the same value of control voltage (V_C = 0.3 V), R_{eq} for FGMOS is 1.30 kΩ whereas it is 1.48 kΩ for QFGMOS-based VCR. The power dissipation of QFGMOS-based VCR (0.04 μW) is less than that of its FGMOS version (0.7 μW).

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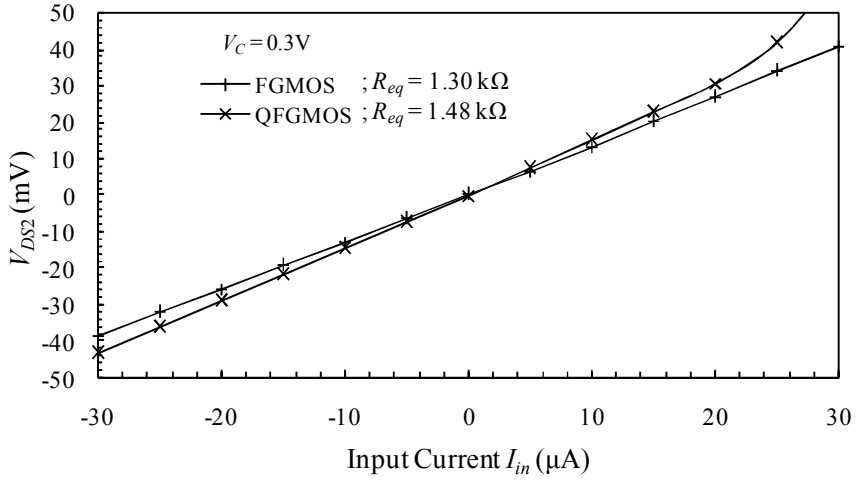

Figure 7. Comparative resistance simulation characteristics

The comparative frequency response of QFGMOS- and FGMOS-based VCRs is shown in Figure 8. The bandwidth of QFGMOS-based VCR is found to be 3.61 GHz, which is greater than that of FGMOS based VCR (490 MHz) due to the absence of large capacitance (C_2).

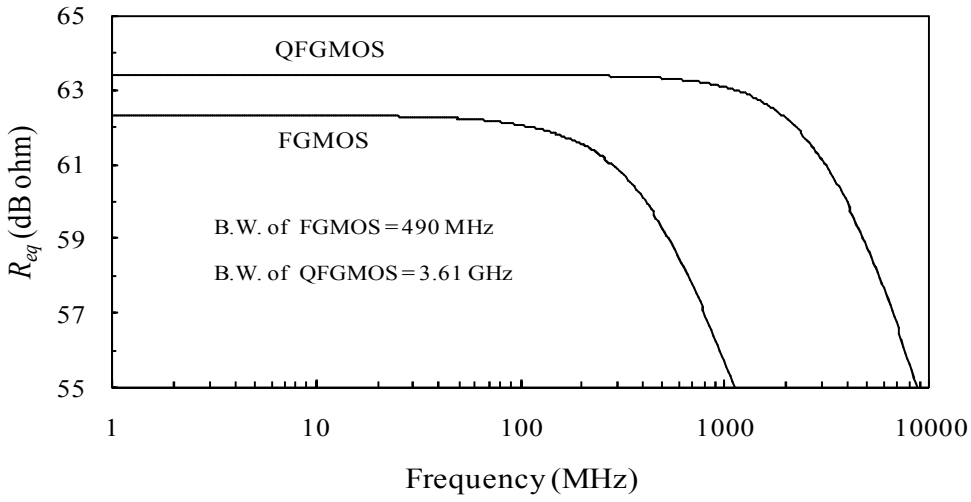

Figure 8. Comparative frequency response of QFGMOS- and FGMOS-based VCRs

CONCLUSIONS

In this paper, we have briefly described QFGMOS and used it to implement a voltage controlled resistor (VCR). The characteristics of QFGMOS-based VCR were compared with those of its FGMOS counterpart. It was found that for a given value of controlling voltage, the QFGMOS-based VCR simulates a higher value of resistance and offers a larger bandwidth as compared to its FGMOS version due to its inherent advantages and consumption of less power. The PSpice simulation results were found to be in conformity with the theory.

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