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Full Paper

Realisation of low-voltage square-root-domain all-pass filters

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Abstract: Novel low-voltage first-order and second-order square-root-domain all-pass filters derived systematically by means of transfer function decomposition and state-space synthesis techniques are proposed. The employment of only a few geometric-mean cells and grounded capacitors permits the circuits to absorb shunt parasitic capacitances, which is desirable for production in monolithic form. The circuits enjoy the features of electronic adjustment of frequency characteristics, wider dynamic range and low-voltage environment operation. The filters are employed to design high-order all-pass filters using cascade approach. First-order low-pass and second-order band-pass filters, being the inherited building blocks of the proposed low-order all-pass filters are also discussed. The behaviour of the filters is evaluated through simulations using Taiwan semiconductor manufacturing company 0.25 µm level-3 complementary metal oxide semiconductor process parameters, where the most important performance factors are considered.

Keywords: analog integrated circuits, companding filters, current-mode circuits, square-root-domain filters, all-pass filters

INTRODUCTION

The downscaling of complementary metal oxide semiconductor (CMOS) processes allows operation of analog-signal processing circuits at relatively reduced voltage levels. The principal motivation for this is to reduce power consumption of the digital circuitry in mixed-mode very large scale integration systems and to prevent gate-oxide breakdown with drop-off in its thickness. In addition, low power consumption and low supply voltages are requirements of the portable electronic equipment. In contrast to the digital circuits, the decrease in the supply voltage of contemporary integrated circuit technologies often necessitates an increase in the power consumption of conventional analog circuit processors for preservation of the same dynamic range and chip area for a given bandwidth [1]. Towards this end, several techniques have been proposed for the reduction of supply voltage in analog and mixed-signal circuits [2-5].

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The technique of companding (compressing-expanding) allows, under low-voltage operating condition, construction of continuous-time analog circuits with higher dynamic range per unit power consumption. In this technique linear input signal is initially compressed before it is handled by the non-linear core system. For preservation of linear operation of the whole system, the non-linear signal produced by the core system is converted to a linear output through employment of an appropriate output stage.

In recent years many researchers have endeavoured to develop companding circuits comprising log-domain and square-root-domain (SRD) topologies [6-25]. However, in most of the integrated circuit (IC) fabrication technologies motivated by the current trend of digital CMOS processes, the more economical metal oxide semiconductor field effect transistor (MOSFET) implementation of log-domain circuits is adopted. To comply with such demand and change, log-domain circuits are designed using strong inversion MOSFETs instead of weak inversion MOSFETs as the circuits based on the latter are sensitive to threshold matching and a mere kilo-hertz-range bandwidth restriction. The problems encountered in the above method were solved by realising SRD filters [13-20]. Since MOSFETs have squared current-voltage (I-V) characteristics in a strong inversion region, derived circuits are therefore known as square-root domains. Thus, the input signal is initially compressed by a square-root operator and in order to preserve the linear operation of the whole system, the non-linear signal produced by the core system is converted back to a linear output signal by employing a squared operator at the output stage. Further, the SRD circuits reduce the fabrication cost, besides eliminating the drawbacks of having high power supply voltage, high-power consumption and low frequency of operation.

The all-pass (AP) filters are among the most important building blocks of many analog signal processing applications and therefore have received due attention. These are generally used for introducing a frequency-dependent delay while keeping the amplitude of the input signal constant over the desired frequency range. During the last few years, some log-domain AP filters were proposed [21, 22]. Some SRD-based AP filters have also been reported in the literature [23-25], although the reported designs are complex, limited to first-order and devoid of electronic tunability feature. Besides, the mathematical modelling is difficult and the effective circuit operation is dependent on transistor matching performance, thus not suitable for monolithic integration. In addition, the reported designs are suited for high voltages and are thus not the candidates for contemporary low-voltage analog and mixed IC design. Based on the above facts, two simple designs for first-order and second-order AP filters are proposed in this paper, which are systematically derived using transfer function decomposition procedure and state-space technique. Compared to various SRD filtering techniques, which require both the geometric mean (GM) cells and the squarer-divider cells for their synthesis, the SRD filter design using state-space technique has the advantage of using only GM cells, resulting in canonical circuit structures with low-power consumption. In addition, the transfer function decomposition procedure, as compared to the direct synthesis, also leads to canonical circuit structures and thus enhances the low-power consumption capability [25]. The functionality of the proposed filters is verified using personal simulation computer programme with integrated circuit emphasis simulations with Taiwan semiconductor manufacturing company 0.25μm CMOS process.

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PROPOSED LOW-VOLTAGE CURRENT-MODE SRD AP FILTER DESIGN

First-Order AP Filter

A first-order AP filter transfer function can be written as:

$$H(s) = k\frac{s\tau - 1}{s\tau + 1} \tag{1}$$

where τ and k are respectively time constant and gain or loss throughout the frequency response of the filter. Equation (1) after decomposition becomes

$$H(s) = k - \frac{2k}{s\tau + 1} \tag{2}$$

The second term in the preceding equation is the transfer function of first-order low-pass (LP) filter for which the state-space equations are:

$$\begin{aligned} \dot{x} &= -\frac{x}{\tau} + 2k\frac{u}{\tau} \\ y &= x \end{aligned} \tag{3}$$

The node voltages, being state variables, permits substitution of x = V_1 and u = U in equation (3) yielding

$$\begin{aligned} \dot{V}_1 &= -\frac{V_1}{\tau} + 2k\frac{U}{\tau} \\ y &= V_1 \end{aligned} \tag{4}$$

Multiplying with constant C on both sides of equation (4), we have

$$\begin{aligned} C\dot{V}_1 &= -C\frac{V_1}{\tau} + 2kC\frac{U}{\tau} \\ y &= V_1 \end{aligned} \tag{5}$$

For a MOSFET in saturated region, the drain current is given by

$$I_{DS} = \frac{1}{2}\mu C_{OX}\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH}\right)^2 = \beta\left(V_{GS} - V_{TH}\right)^2 \tag{6}$$

where β, V_{GS} and V_{TH} are transconductance parameter, gate to source voltage and threshold voltage of the MOSFET respectively. The new currents I_1, I_U and I_o are defined as

$$\begin{aligned} I_1 &= \beta\left(V_1 - V_{TH}\right)^2 \Rightarrow V_1 = \sqrt{\frac{I_1}{\beta}} + V_{TH} \\ I_U &= \beta\left(U - V_{TH}\right)^2 \Rightarrow U = \sqrt{\frac{I_U}{\beta}} + V_{TH} \end{aligned} \tag{7}$$

$$I_o = \frac{C^2}{\tau^2\beta} \Rightarrow \tau = \frac{C}{I_o\beta} \tag{8}$$

After routine manipulation, the state-space equations become

$$\begin{aligned} C\dot{V}_1 &= 2k\sqrt{I_o I_U} - \sqrt{I_o I_1} + I_T\left(2k - 1\right) \\ y &= V_1 \end{aligned} \tag{9}$$

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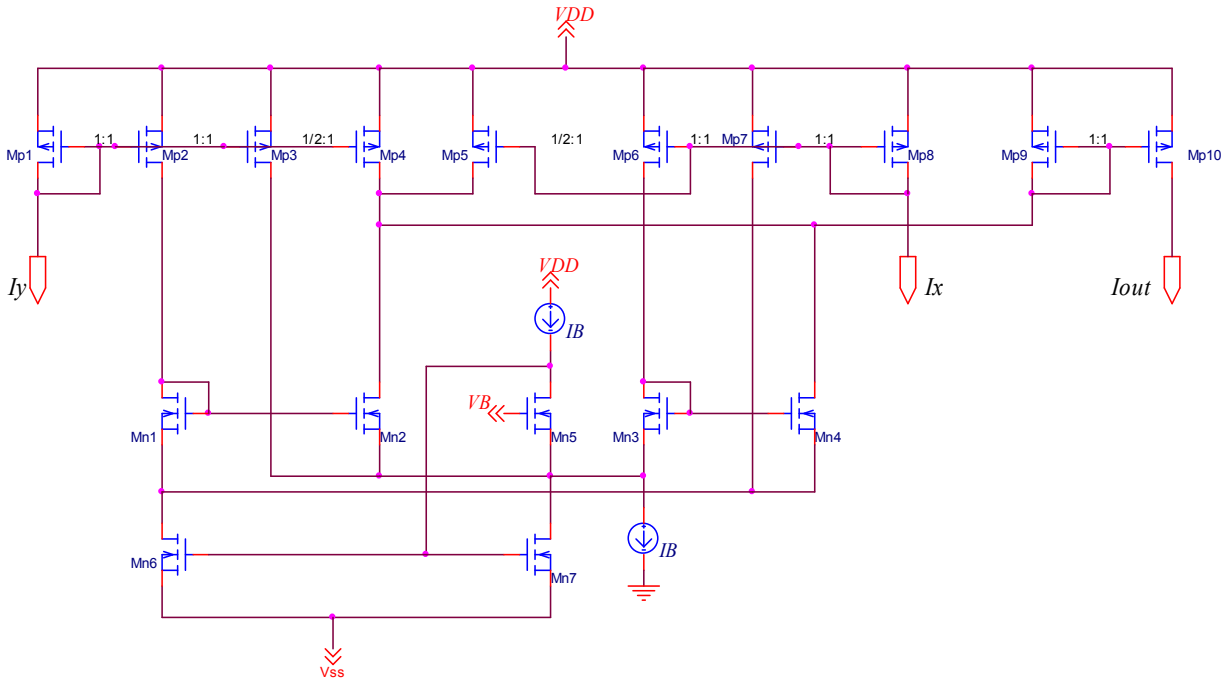
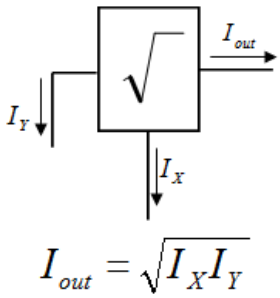
where

$$I_T = \frac{CV_{TH}}{\tau} = V_{TH}\sqrt{I_o\beta} \tag{10}$$

Equation (9) is the complete derivation of the first-order LP filter. An examination of equation (9) reveals that it can be transformed into a circuit through interconnection of two square-root circuits, a load capacitor, some current mirrors, two additional DC-biased current sources and two n-type MOSFETs. From equation (9), it is clear that for the implementation of the proposed LP filter, a square-root circuit or GM cell is needed. According to our literature survey, among the various GM cells, the most commonly used one is given in Figure 1 [26] as it has a low-voltage requirement. The complete circuit diagram of the proposed first-order AP filter constructed as per equations (2) and (9) is as shown in Figure 2.



(a)



(b)

Figure 1. (a) Low-voltage current GM cell; (b) The employed symbols

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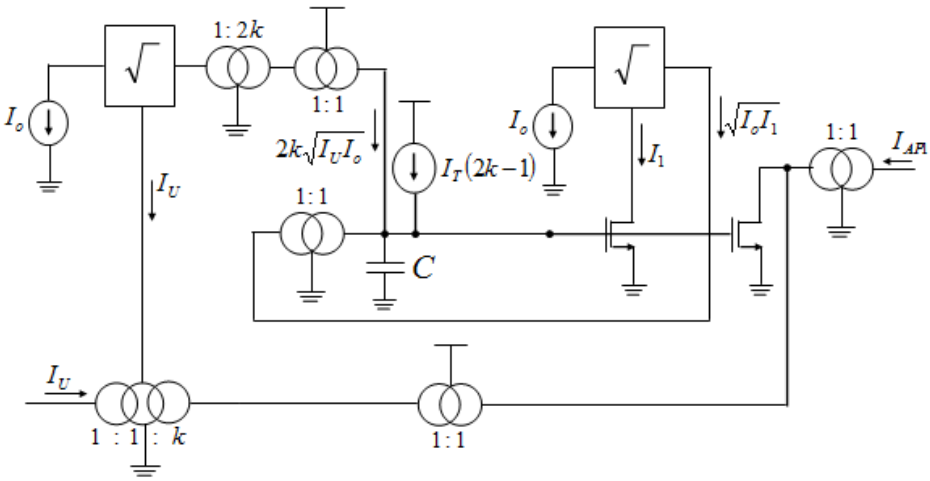

Figure 2. Proposed low-voltage SRD design of first-order AP filter

Second-Order AP Filter

The transfer function for second-order AP filter can be written as:

$$H(s) = k\frac{s^2\tau^2 - \frac{s\tau}{Q} + 1}{s^2\tau^2 + \frac{s\tau}{Q} + 1} \tag{11}$$

This after decomposition becomes

$$H(s) = \frac{Y(s)}{U(s)} = k - \frac{2k\frac{s\tau}{Q}}{s^2\tau^2 + \frac{s\tau}{Q} + 1} \tag{12}$$

The transfer function of the second-order band-pass filter is represented by the second term of the preceding equation. By following a similar procedure as introduced the pervious section, the complete derivation of the second-order band-pass filter is

$$\begin{aligned} C\dot{V}_1 &= -\sqrt{I_o I_2} - I_T \\ C\dot{V}_2 &= \sqrt{I_o I_1} - \frac{\sqrt{I_o I_2}}{Q} + 2k\frac{\sqrt{I_o I_U}}{Q} + I_S \\ y &= V_2 \end{aligned} \tag{13}$$

where

$$I_S = I_T\left(1 + \frac{2k}{Q} - \frac{1}{Q}\right) \tag{14}$$

Equation (13) can be implemented in circuit form through the use of three GM cells, two grounded capacitors, several current mirrors, three additional DC-biased current sources and three n-type MOSFETs. The proposed second-order AP filter obtained by means of equations (12) and (13) is as depicted in Figure 3. Moreover, a high-order AP filter can be implemented by cascading

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low-order (first-order and second-order) AP filters and the same has been verified with the help of simulated results.

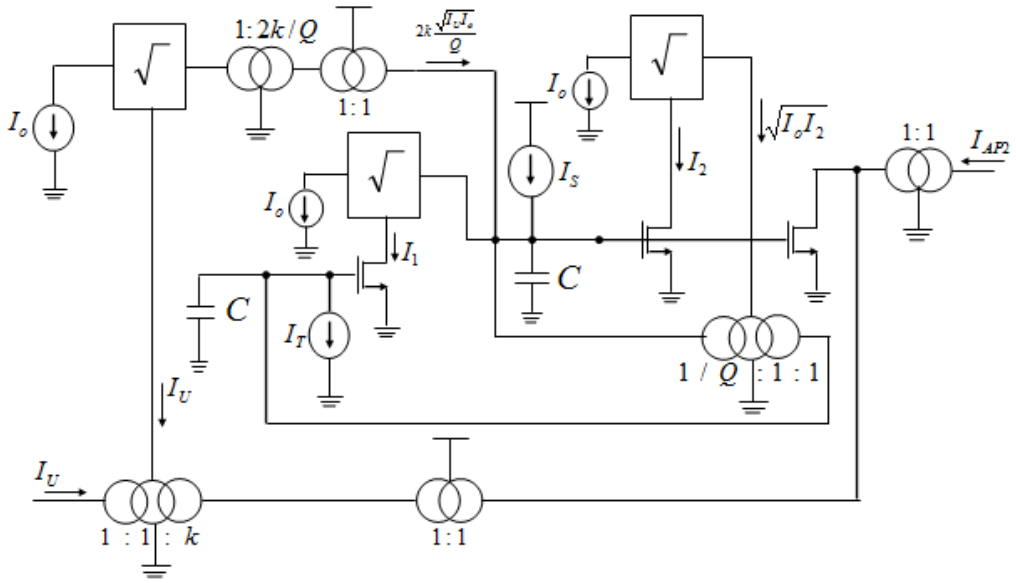

Figure 3. Proposed low-voltage SRD design of second-order AP filter

SIMULATION RESULTS

In order to verify the theoretical predictions contained in the previous section, the proposed low-order AP circuits shown in Figures 2 and 3 are simulated using Taiwan semiconductor manufacturing company 0.25µm CMOS process parameters. For both the filters, the aspect ratio of transistors used in the current mirror is W/L = 20µm/2µm and those used in the GM cell are given in Table 1.

Table 1. Aspect ratios of metal oxide semiconductor (MOS) transistors of GM cell

Transistor	W/L (µm/µm)
M_{p1}-M_{p3}	11.6/2
M_{p4}	5.8/2
M_{p5}	14/2
M_{p6}-M_{p10}	28/2
M_{n1}-M_{n4}	3.6/2
M_{n5}	20/2
M_{n6}-M_{n7}	30/2
M_{n8}-M_{n9}	10/2

The simulated value of pole frequency is found to be 100 kHz for V_{DD} = 1.5 V, V_{SS} = 0V, C_1 = C_2 = 56.27pF and I_0 = 5µA. Figures 4 and 5 depict the simulated magnitude and phase responses of first- and second-order AP filters respectively. Furthermore, the simulated frequency responses of LP and band-pass filters, the intrinsic building blocks of the low-order and high-order AP filters, are shown in Figure 6. The simulated phase responses obtained from low-order AP filters of Figures 2 and 3 are shown in Figure 7. It is worth mentioning here that the simulated ideal curves

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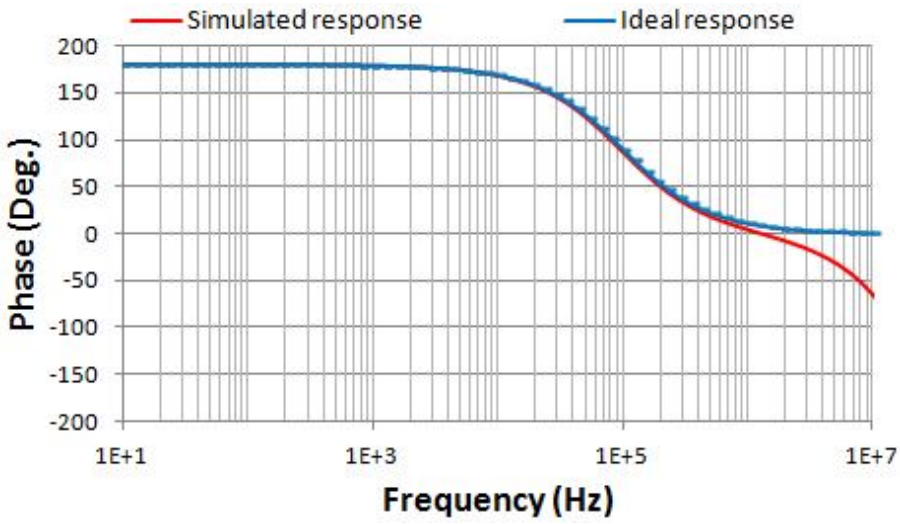
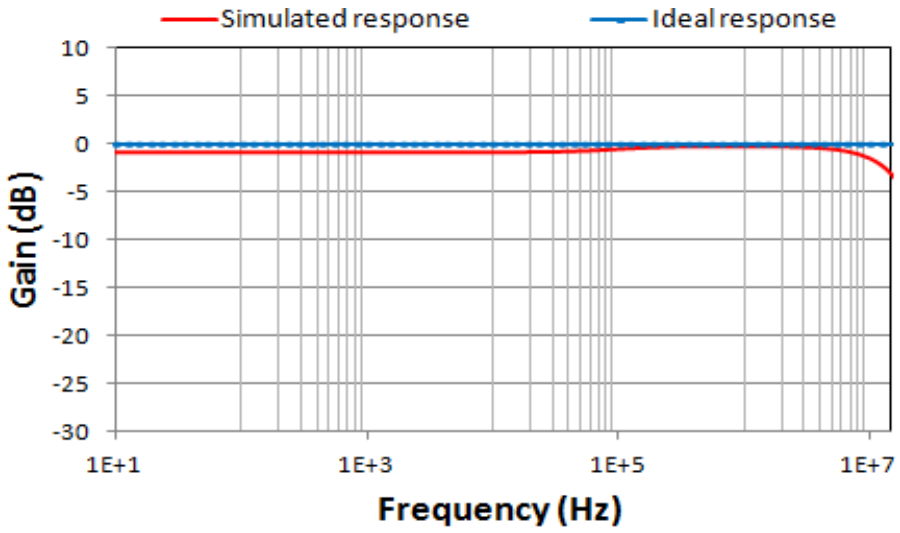
of Figure 7 were obtained by implementing equations (1) and (11) using ideal voltage-controlled current sources with the same set of coefficients as those chosen for the SRD design.



(a)



(b)

Figure 4. Simulated responses of first-order AP filter: (a) magnitude response; (b) phase response

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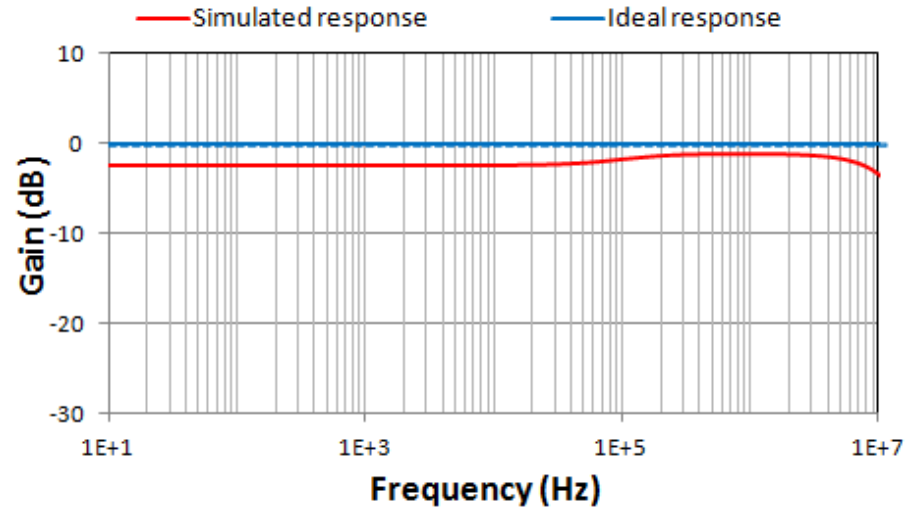
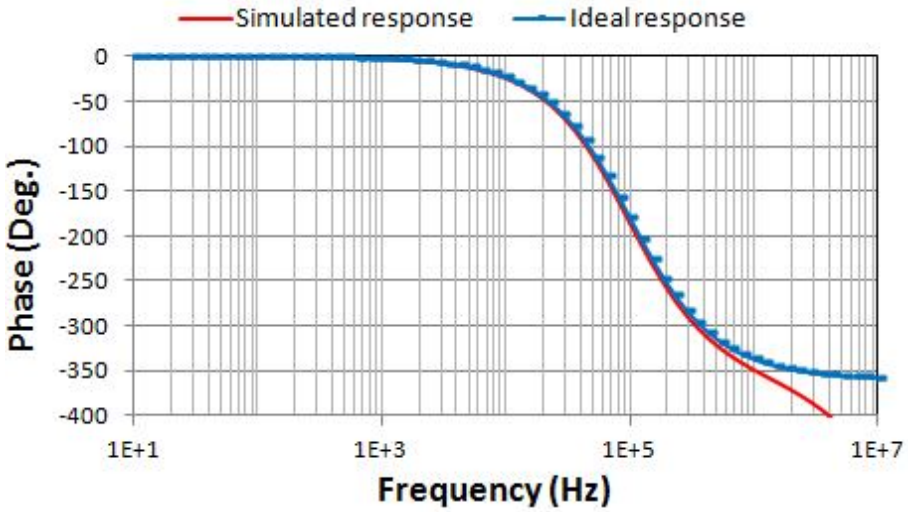


(a)



(b)

Figure 5. Simulated responses of second-order AP filter: (a) magnitude response; (b) phase response

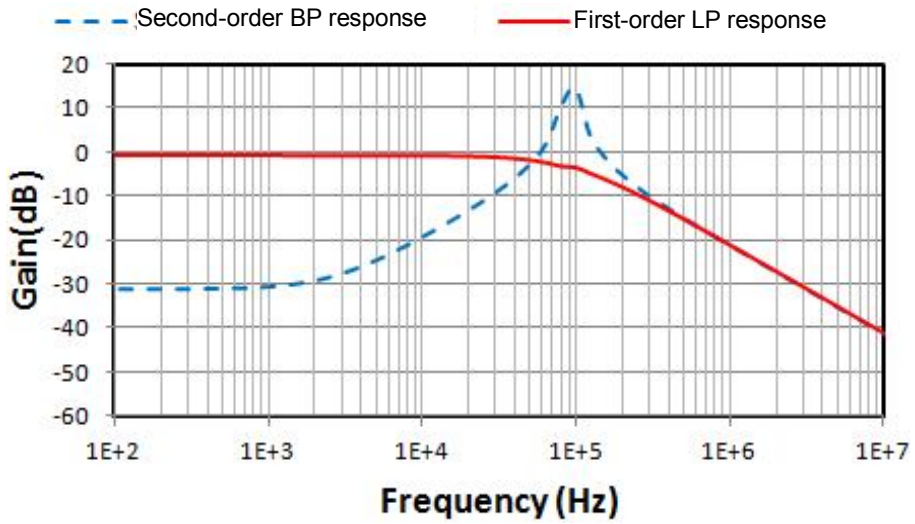


Figure 6. Simulated magnitude responses of first-order LP filter and second-order band-pass filter

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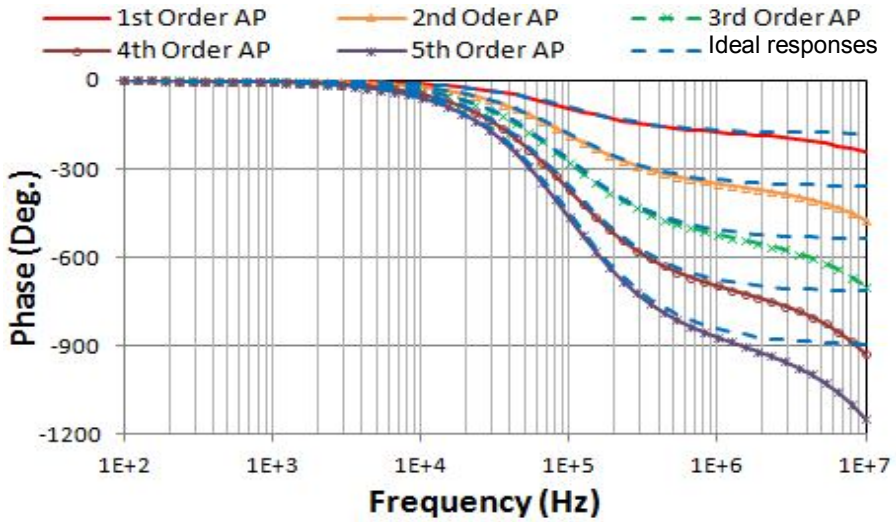

Figure 7. Simulated phase responses of higher-order AP filters

To demonstrate the electronic tunability of the proposed circuits, I_0 was varied and the results obtained for 1.25µA, 5µA and 20µA are depicted in Figure 8. Additionally, the performance of the proposed AP filters was evaluated for the parameters of linearity, noise and mismatching. The obtained results are summarised in Table 2.

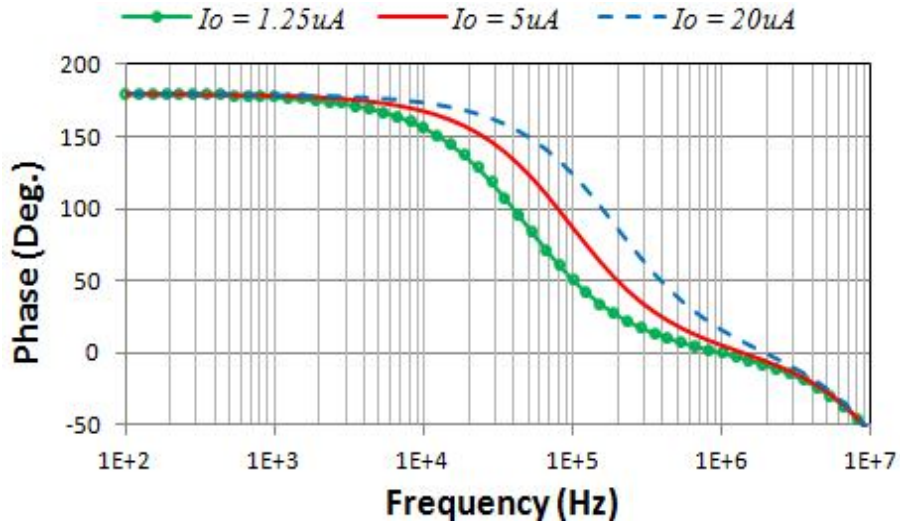

Figure 8. Demonstration of electronic tunability of the proposed AP designs

Table 2. Performance factor results for the proposed AP filters

Performance factor	Value		
	1st-Order AP	**2nd-Order AP**	**5th-Order AP**
Power dissipation	250µW	475µW	1.03mW
Dynamic range	49.2dB	48.7dB	47.1dB
Sensitivity of ω_0	76.4kHz	79.4kHz	83.5kHz

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CONCLUSIONS

Novel low-voltage SRD first-order and second-order AP filter structures having electronic tunability feature and amenability for monolithic integration are presented. A systematic synthesis procedure for deriving the filter circuits together with their use in the design of high-order AP filters is also given. The circuits, besides consuming low power, consist merely of a few SRD cells and grounded capacitors.

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