Full Paper

Protective coordination of main and backup overcurrent relays with different operating modes of active super-conducting current controller

Ahmad Ghafari [*], **Morteza Razaz, Ghodratollah Seifossadat** and **Mohsen Hosseinzadeh Soreshjani**

Department of Electrical Engineering, Shahid Chamran University of Ahvaz, Ahvaz, Iran

* Corresponding author, e-mail: ghafari.ieee@gmail.com

Abstract: Active superconducting current controllers (ASCCs) are new generation of series compensators, which can also be categorised as fault current limiters because of their ability to decrease the fault current continuously. Although the performance of the ASCCs in different operating modes introduces a limiting impedance in series with the network, it can degrade the operation of the overcurrent relays (OCRs). In this paper the ASCC modelling and its control strategy for fault detection and converter operation is investigated. The simulation of a typical three-phase ASCC shows the effect of the ASCC on fault current limiting and confirms the operation of the control system. The impact of different modes of ASCC on the operation of the main and backup OCRs is studied through the simulation of a typical distribution system. Simulation results confirm that the protective coordination of different modes of the ASCC is achieved by modifying both the time dial and pickup current parameters of the OCRs.

Keywords: current controller, fault current limiters, main and backup protection, overcurrent relay, power distribution system, superconducting devices

INTRODUCTION

The recent growth of electrical energy demand and the rapid development of the power systems have increased short-circuit phenomena which can damage circuit breakers and other equipment. The application of fault current limiters (FCLs) can be regarded as an effective solution for this issue [1]. Several researches have introduced and evaluated different types of FCLs. For example, the resistive, magnetic-shield, high-temperature superconducting, saturated iron-core, and shunt superconducting FCL types have been presented and examined [2-5]. In general, these types

of FCLs have a low resistance against the line current under the normal state, but they suddenly represent a large resistance against the current when a fault occurs.

The active superconducting current controller (ASCC) as a new generation of series compensations is a combination of superconductor technology and power electronic devices [6]. This type of superconducting FCL can decrease the fault current continuously at different levels. In addition, it can also be implemented in the hybrid alternating-current-to-direct-current (AC-DC) power supply systems [7-8]. In spite of the aforementioned advantages, the ASCC may deteriorate the operation of employed over-current relays (OCRs). It stands to reason that reducing the fault current increases the trip time of the OCR and may deteriorate the transient stability of the network. The ASCC has been applied to reduce the fault current in the presence of a transformer rating of 100 megavolt-amperes to a level of normal current when a 45-megavolt-ampere transformer is used [9]. Although the protective coordination of the main relay has been considered [9], there seems to be no study of the protective coordination of both the main and backup OCRs. Thus, the main aim of this work is to analyse the protective coordination of the main and backup OCRs with adjustment of both the ASCC and OCR parameters to obtain a state of ASCC setting that can achieve simultaneously its most current-limiting capability and protective coordination.

NOTATIONS

L_1, M_S : Self- and mutual-inductances of ASCC

U_A, I_A : Superconducting transformer phase-A primary voltage and current in a transmission system

U_a, I_a : Superconducting transformer phase-A secondary voltage and current in a transmission system.

U_{SA} : Voltage source of phase A

Z_1, Z_2 : Line and load impedances

$I_{Af\text{-}withASCC}, I_{Af\text{-}noASCC}$: Fault current with and without ASCC

$I_{Af\text{-}1}, I_{Af\text{-}2}, I_{Af\text{-}3}$: Fault current in modes 1, 2 and 3

$Z_{ASCC\text{-}1}, Z_{ASCC\text{-}2}, Z_{ASCC\text{-}3}$: Limiting impedance of ASCC in modes 1, 2 and 3

K : Coefficient constant

$Z_{ASCC\text{-}F}, Z_{ASCC\text{-}N}$: Limiting impedance of ASCC in fault and normal states

Z_T^1, Z_T^2, Z_T^0 : Equivalent impedance of positive, negative and zero sequences

$Z_{ASCC}^1, Z_{ASCC}^2, Z_{ASCC}^0$: ASCC impedance of positive, negative and zero sequences

C_1, C_2 : Split DC link capacitors

L_d, C_d : Filtering inductance and capacitor

i_d, i_q, i_0 : Instantaneous system current in synchronous reference frame

$i_{d\text{-}ref}, i_{q\text{-}ref}, i_{0\text{-}ref}$: Steady-state system current in synchronous reference frame

Δi : Amplitude of error between the instantaneous and steady-state current

A, B, P : Constants of a relay

TD : Time Dial of OCR

M : Multiple of current

I_{input}, I_p : Fault current and pickup current of OCR

ω : Angular frequency of source voltage

j : Index of imaginary numbers, which is equal to the square root of -1

CONFIGURATION AND MODELLING

Structure and Principle of ASCC

The ASCC structure for a typical three-phase circuit (Figure 1) consists of three superconducting transformers and one three-phase pulse-width-modulation (PWM) converter. In the normal state, the limiting impedance of the ASCC is adjusted to zero, but in the fault conditions it is increased through controlling the output current of the converter. Consequently, the fault current is limited to different levels [10-13].
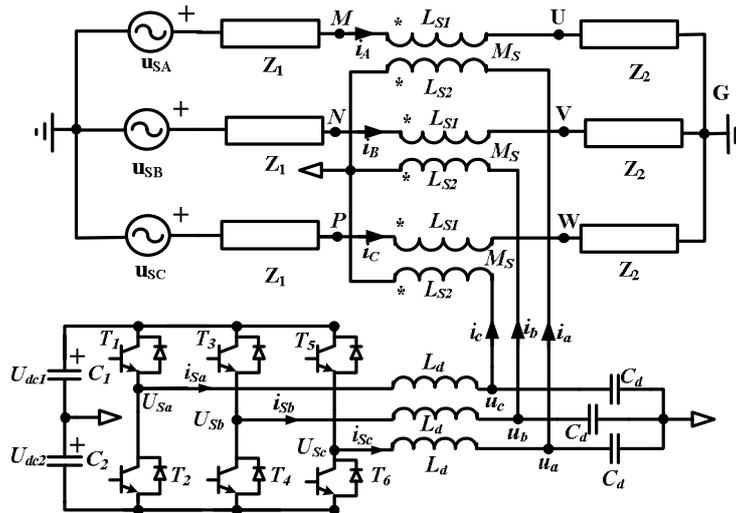
Figure 1. Structure of a three-phase ASCC

In this paper, phase A shown in Figure 1 is studied for the sake of simplicity of modeling, and the other two phases can be analysed in the same way. The primary voltage of the super-conducting transformer is expressed as follows [6, 11-13].

$$U_A = j\omega L_{S1} I_A - j\omega M_S I_a \tag{1}$$

where L_{S1} is defined as:

$$L_{S1} = L_1 + M_S \tag{2}$$

In the normal state, I_a should be adjusted as:

$$I_a = \frac{L_{S1}}{M_S} I_A = \frac{L_{S1}}{M_S} \left(\frac{U_{SA}}{Z_1 + Z_2} \right) \tag{3}$$

When a fault occurs, the fault current without ASCC and with ASCC is defined as:

$$I_{Af-noASCC} = \frac{U_{SA}}{Z_1} \tag{4}$$

$$I_{Af-withASCC} = \frac{U_{SA} + j\omega M_S I_a}{Z_1 + j\omega L_{S1}} \tag{5}$$

In addition, the limiting impedance of ASCC (Z_{ASCC}) is defined as:

$$Z_{ASCC} = \frac{U_{Af}}{I_{Af}} = j\omega L_{S1} - \frac{j\omega M_S I_a (Z_1 + j\omega L_{S1})}{U_{SA} + j\omega M_S I_a} \tag{6}$$

Based on (5), three different modes are defined for the operation of ASCC [6-8]:

Mode 1: I_a is kept at the original setting, and

$$I_{Af-1} = \frac{U_{SA} + j\omega L_{S1} I_A}{Z_1 + j\omega L_{S1}} \tag{7}$$

$$Z_{ASCC-1} = \frac{Z_2(j\omega L_{S1})}{Z_1 + Z_2 + j\omega L_{S1}} \tag{8}$$

Mode 2: The amplitude of I_a is set at zero, and

$$I_{Af-2} = \frac{U_{SA}}{Z_1 + j\omega L_{S1}} \tag{9}$$

$$Z_{ASCC-2} = j\omega L_{S1} \tag{10}$$

Mode 3: I_a is adjusted so that the measured angle between u_{SA} and $j\omega M_s I_a$ is equal to 180°, and this is obtained by setting $j\omega M_s i_{2a} = -K u_{SA}$. In this mode, the limiting impedance is defined as:

$$I_{Af-3} = \frac{U_{SA} - \omega M_S |I_a|}{Z_1 + j\omega L_{S1}} \tag{11}$$

$$Z_{ASCC-3} = \frac{K}{1-K} Z_1 + \frac{1}{1-K} j\omega L_{S1} \tag{12}$$

In order to investigate the ASCC performance for asymmetric faults, it is assumed that a phase-A-to-ground fault occurs. The limiting impedance of phase A is therefore adjusted to the fault state impedance of modes 1, 2 and 3, and the limiting impedance for other phases is kept at its normal state. The voltage and current equations are thus expressed as:

$$V^{abc} = Z^{abc} I^{abc} \tag{13}$$

where

$$Z^{abc} = \begin{bmatrix} Z_{ASCC-F} & 0 & 0 \\ 0 & Z_{ASCC-N} & 0 \\ 0 & 0 & Z_{ASCC-N} \end{bmatrix}.$$

The zero-, positive- and negative-sequence components of phase A are obtained as:

$$Z^{012} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix} \begin{bmatrix} Z_{ASCC-F} & 0 & 0 \\ 0 & Z_{ASCC-N} & 0 \\ 0 & 0 & Z_{ASCC-N} \end{bmatrix} \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \tag{14}$$

where $a = 1\angle120°$, $a^2 = 1\angle240°$.

If a single-phase fault occurs, the fault current of positive, negative and zero sequences will be equal, and they are calculated as:

$$I_F^0 = I_F^1 = I_F^2 = \left(\frac{U_{SA}}{Z_T^1 + Z_T^2 + Z_T^0 + 3Z_f} \right) \tag{15}$$

In (15), Z_T^1, Z_T^2 and Z_T^0 are the equivalent impedance of positive, negative and zero sequences, which are defined as:

$$\begin{cases} Z_T^1 = Z_S + Z_{Tr} + Z_{ASCC}^1 \\ Z_T^2 = Z_S + Z_{Tr} + Z_{ASCC}^2 \\ Z_T^0 = Z_S + Z_{Tr} + Z_{ASCC}^0 \end{cases} \tag{16}$$

The fault current of positive, negative and zero sequences ($I^1{}_F$, $I^2{}_F$ and $I^0{}_F$) for two-phase and two-phase-to-ground faults are obtained by (17) and (18) respectively:

$$\begin{cases} I_F^0 = 0 \\ I_F^1 = -I_F^2 = \left(\dfrac{\dot{U}_{SA}}{Z_T^1 + Z_T^2 + Z_f} \right) \end{cases} \tag{17}$$

$$\begin{cases} I_F^0 = 0 \\ I_F^1 = -I_F^2 = \left(\dfrac{\dot{U}_{SA}}{Z_T^1 + \dfrac{Z_T^2 \left(Z_T^0 + aZ_f \right)}{Z_T^2 + Z_T^0 + aZ_f}} \right) \end{cases} \tag{18}$$

Control Strategy for Fault Detection and Voltage Source Converter

The control strategy for fault detection is illustrated in Figure 2. For the sake of simplicity of the design, the currents are expressed in the synchronous reference frame. In order to detect the normal and fault conditions, instantaneous currents (i_d, i_q and i_0) and steady-state currents ($i_{d\text{-}ref}$, $i_{q\text{-}ref}$ and $i_{0\text{-}ref}$) are compared. If $\Delta i > \Delta i_{threshold}$, a fault occurs, and the ASCC provides the required compensating voltage to control the fault current level [1].

In addition, the control system diagram of a three-phase converter is shown in Figure 3. The reference current signals ($i_{abc\text{-}ref}$) are determined based on the operating state of the main circuit and the current-limiting mode of the ASCC. Consequently, the reference currents and voltages are calculated. Finally, the voltage reference signals of the converter can be obtained by *dq0-abc* transformation [11].

Distribution System

In a number of research work [14-17], the system used by the Korea Electric Power Corporation was chosen for investigation in the presence of superconducting fault current limiters since it contains both main and backup protections. So this system is selected here as the case study. The ASCC employed in this system is depicted in Figure 4. R_1-R_5 are OCRs that protect the related feeders of the distributed system, and R_6 is used not only as the main protection for the transformer, but also as the backup protection for R_1 - R_5. In turn, R_7 is employed as the backup protection for R_6. The parameters of the distribution system, along with the initial settings of the OCRs, are shown in Table 1 [16].
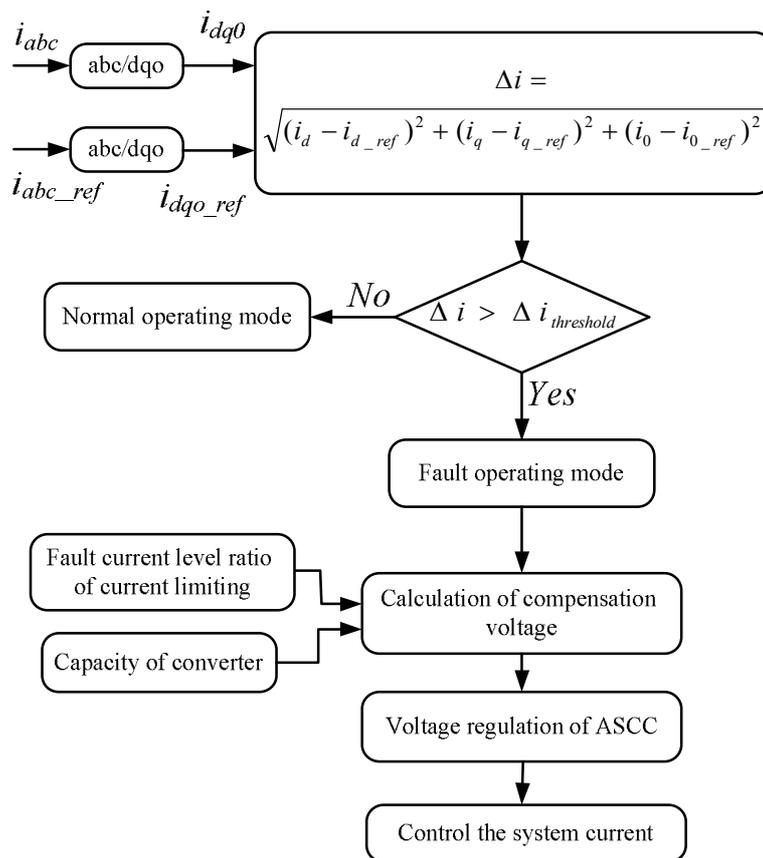
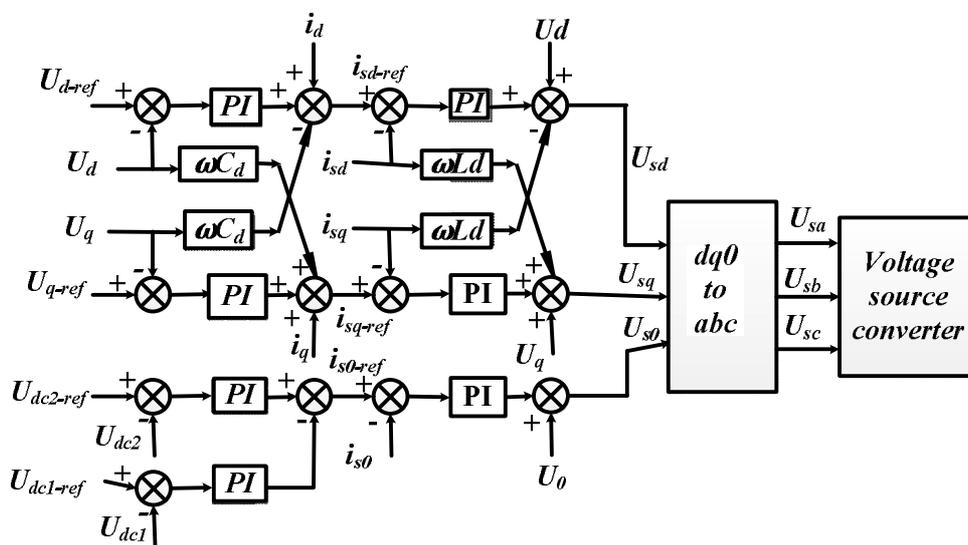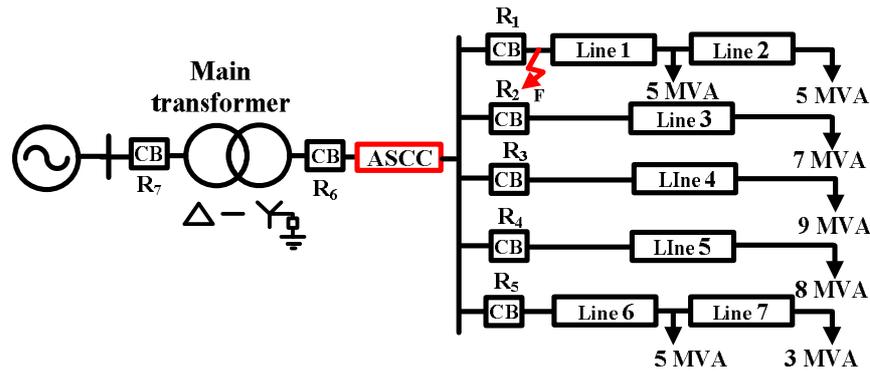**Figure 2.** Control strategy for fault detection

Figure 3. Control strategy for a three-phase pulse-width-modulation converter

Figure 4. Schematic configuration of the distribution system

Table 1. Detailed specifications of distribution system and OCR

Configuration components	Specification
Source	154 (KV) , 1.75%
Transformer	154/22.9 (KV), 100 (MVA) , j 20(%)
Distribution line	Z_0=8.68+j22.86 (%) , (100MVA) Z_1=Z_2 =3.48+j7.44 (%) , (100MVA)
Loads	Feeder1: 10 (MVA) , pf=0.95 Lag Feeder2: 7(MVA) , pf=0.95 Lag Feeder3: 9 (MVA) , pf=0.95 Lag Feeder4: 8 (MVA) , pf=0.95 Lag Feeder5: 8 (MVA) , pf=0.95 Lag
OCR	Load current: 1.13 (KA$_{rms}$) Full load current: 1.51 (KA$_{rms}$) Pick-up current of time delay operation: 2.1 (KA$_{rms}$) Level: 1
	Parameters of very-inverse-type OCR: *A*=3.88, *B*=0.0963, *P*=2, *TD*=0.4
Superconducting FCL parameters	L_{s1}=L_{s2}=5 (mH), M_s=4 (mH)

Modelling of OCR

For the modelling purpose, the operational equations of OCR are obtained as follows [16]:

$$Time_{trip} = (\frac{A}{M^P - 1} + B) * TD \tag{19}$$

$$M = \frac{I_{input}}{I_{pickup}} \tag{20}$$

where *A*, *B* and *P* are determined based on the type of relays. According to (20), I_{input} is equal to the fault current and I_{pickup} is one of the setting parameters of OCR. *TD* is another setting parameter of OCR. By adjusting *TD* and I_{pickup} through analysis of the time-current curve, the protective coordination of ASCC with OCR is obtained for different current limiting modes. According to (7) - (11), the operational equations of OCR without ASCC and in the presence of ASCC are obtained as follows:

$$\begin{cases} (Time_{trip})_{WITHOUT-ASCC} = (\dfrac{A}{(\dfrac{U_{SA}}{Z_1 I_{pick-up}})^P - 1} + B) * TD \\[4ex] (Time_{trip})_{ASCC-1} = (\dfrac{A}{(\dfrac{U_{SA} + j\omega L_{S1} I_A}{(Z_1 + j\omega L_{S1}) I_{pick-up}})^P - 1} + B) * TD \\[4ex] (Time_{trip})_{ASCC-2} = (\dfrac{A}{(\dfrac{U_{SA}}{(Z_1 + j\omega L_{S1}) I_{pick-up}})^P - 1} + B) * TD \\[4ex] (Time_{trip})_{ASCC-3} = (\dfrac{A}{(\dfrac{U_{SA} - \omega M_S |I_a|}{(Z_1 + j\omega L_{S1}) I_{pick-up}})^P - 1} + B) * TD \end{cases} \qquad (21)$$

Equations (21) show that reducing the fault current increases the trip time of OCR so that ASSC with mode 3 provides the largest trip time of OCR (i.e. $(Time_{trip})_{ASCC-3} > (Time_{trip})_{ASCC-2} > (Time_{trip})_{ASCC-1}$). This increase in the relay operation may therefore deteriorate the transient stability. For this reason, the protective coordination between ASCC and OCR for the whole modes of ASCC is inevitable, and this is performed through the setting of OCR parameters.

SIMULATIONS AND RESULTS

In order to evaluate the effect of different modes of ASCC on current limiting, a simulation of the three-phase circuit shown in Figure 1 was performed. In addition, to study the protective coordination of the main and backup relays by considering all different modes of ASCC, a simulation of the distribution system depicted in Figure 4 was also carried out.

Current Limiting Test

To assess the performance of the three aforementioned modes of ASCC on current limiting, the model shown in Figure 1 with parameters as in Table 2 was simulated in MATLAB. In order to evaluate and compare the effects of different modes of ASCC on current limiting, the fault current waveforms with and without ASCC are compared (Figure 5), which shows that ASCC can reduce the fault current as expected. In addition, by adjusting the phase angle of output current of the converter to 90° (i. e. mode 3), the maximum effect of fault-current limiting is obtained.

Table 2. Parameters of simulated system

Parameter	Value
$[U_{SA}, U_{dc}]$	[220,600] (V)
Z_1	0.19 + 2.16 i (Ω)
Z_2	15 + 2 i (Ω)
F	50 (Hz)
$Ls_1 = Ls_2$	10 (mH)
$[M_s, L_f]$	[9, 6] (mH)
$C_1 = C_2$	2000 (μF)
C_f	30 (μF)
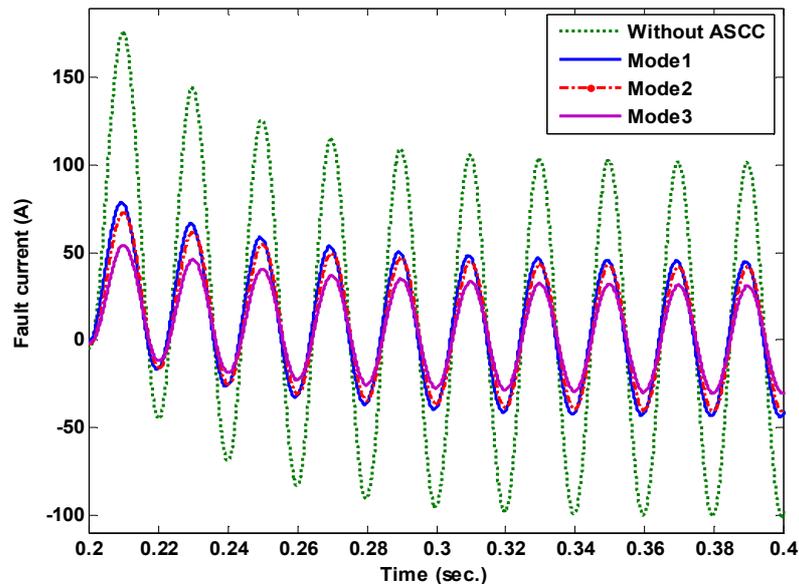
Figure 5. Comparison of fault current characteristics

By supposing the operation of ASCC in mode 3, the voltage and current reference signals of the converter under different conditions, viz. normal state, three-phase fault and single-phase fault, are shown in Figure 6. Figure 6a shows the reference currents of the normal state. The reference current of phase A can be obtained based on equation (3), and reference currents of the other phases (B and C) are the same as that of phase A due to symmetrical conditions (I_{a-ref}=15.7$\angle$-15.3°, I_{b-ref}= 15.7$\angle$-135.3° and I_{c-ref}=15.7$\angle$104.3°). In Figure 6b, the reference current of phase A is 15.7$\angle$90° since the ASCC operates in mode 3. Consequently, due to a symmetrical fault, I_{b-ref} and I_{c-ref} are equal to 15.7$\angle$-30° and 15.7$\angle$-150° respectively. In Figure 6c, as a result of the operation of ASCC in mode 3, the current of phase A is 15.7$\angle$90°, and because of an unsymmetrical fault, I_{b-ref}= 15.7$\angle$-135.3° and I_{c-ref}=15.7$\angle$104.3° are obtained similar to the normal state. In addition, when the single-phase fault occurs, the AC components of DC link voltage of the converter (U_{dc1} and U_{dc2}) are opposite to each other, and the total DC voltage is kept at the level of 600 V.

Figure 7 depicts the current and voltage waveforms of the superconducting transformer in the presence of the ASCC. Interval t = 0.2-0.23 sec. is the time for detecting the fault for the operation of the converter, and the line current is reduced to 44.38 A since the ASCC operates in mode 1. Similarly, from t = 0.23 sec. to 0.4 sec., by setting the phase angle of compensating current (I_a) to 90°, defined as mode 3, the fault current is reduced to 30.76 A. It is notable that when a fault occurs, the fault current is suddenly reduced to a suitable level when the ASCC with its original setting operates in mode 1. After fault detection, based on the converter's control strategy, the ASCC operates in mode 3, causing the maximum effect on current limiting. In other words, the operating modes of the ASCC are selected based on the reference signals.
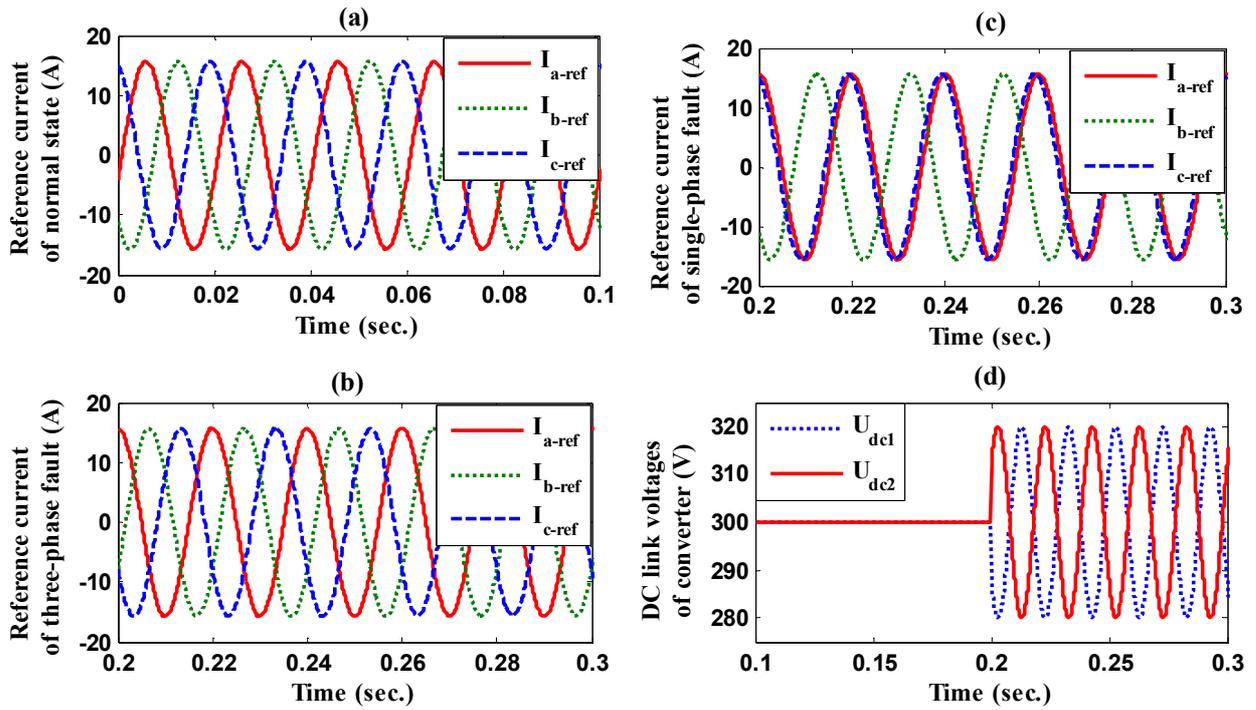
Figure 6. Reference current of normal state (a), three-phase fault (b) and single-phase fault (c), and dc link voltage of converter for single-phase fault (d)
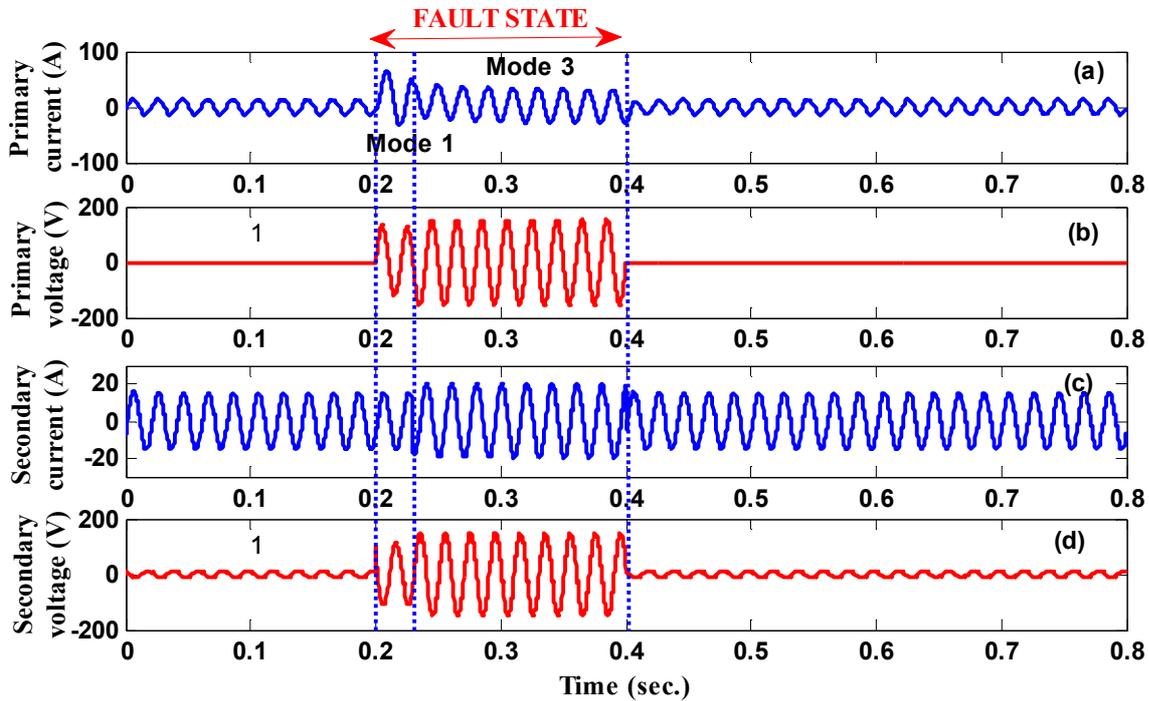

Figure 7. Waveforms of superconducting transformer: (a) primary current (I_A); (b) primary voltage (U_A); (c) secondary current (I_a); (d) secondary voltage (u_a)

Operation of OCRs

In the first state, the operation of one relay (R_6) was investigated and its appropriate setting parameters for the protective coordination in the whole modes of ASCC were calculated. Then the protective coordination of the whole relays, illustrated in Figure 4, was evaluated. For different

operating modes of ASCC, the time-current curve of the OCR is shown in Figure 8. To meet the protective coordination in modes 1 and 2, the modification of *TD* value from '0.5' to '0.1' is inevitable. The operation times of OCR in this case are reduced to 0.27 sec. and 0.3 sec. respectively. When the ASCC operates in mode 3 and *TD* is equal to '0.1', the operation time of OCR is 0.57 sec. and thus, in this mode adjusting the other setting parameter of OCR (I_{pickup}) is necessary. According to Figure 8d, when the *TD* value of OCR changes from '0.5' to '0.1' and I_{pickup} is also modified from '2.1' to '1.9', the protective coordination in three operation modes is performed. Based on equation (5), in mode 3, when the amplitude of output current of the converter is increased, the current limiting further decreases, and consequently the protective coordination cannot be achieved even by adjusting the OCR parameters to their minimum values.
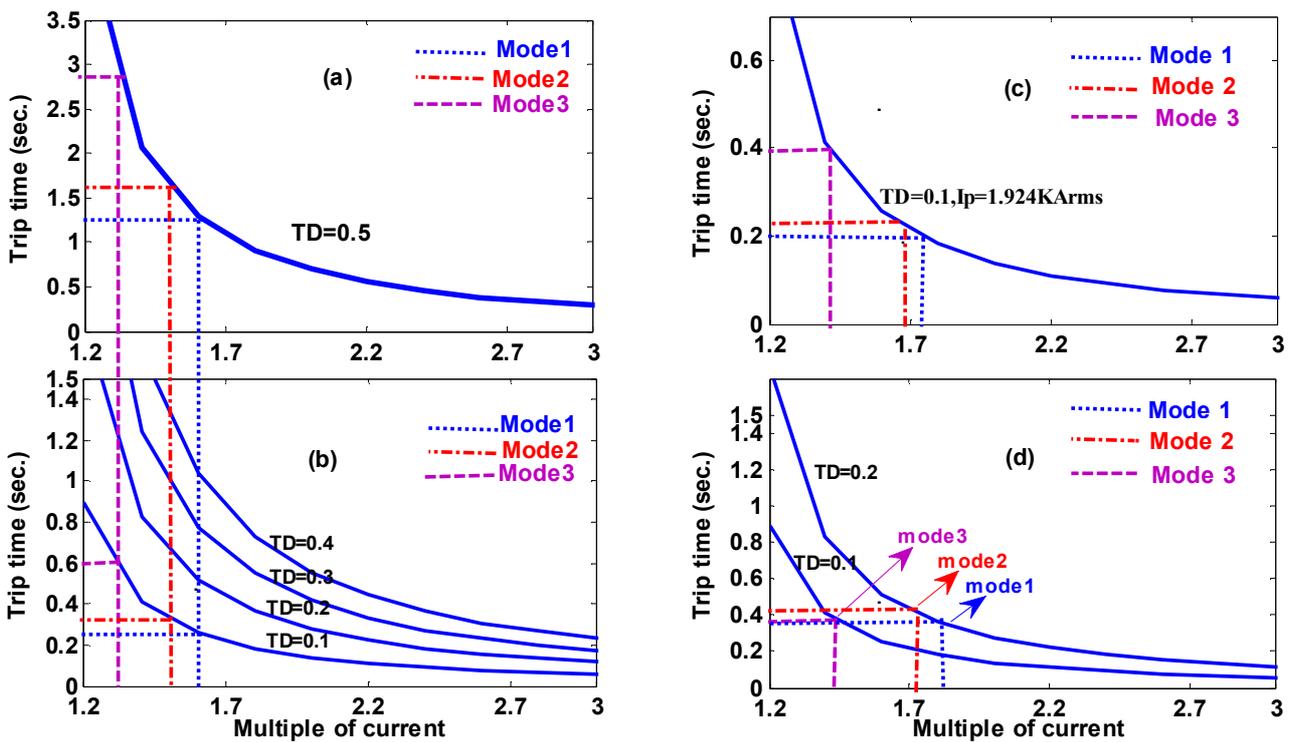
Figure 8. Time-current curve of OCR operation for the protective coordination with ASCC operation: (a) original settings of OCR; (b) Coordination with modified *TD*; (c) Coordination by modifying both *TD* and I_p for mode 3; (d) Coordination by modifying both *TD* and I_p for modes 1-3

In the second state, to study the protective coordination of the whole OCRs, simulations consisting of 27 cases of coordination (nine protective states and three modes of ASCC) were considered. The values of rated current (I_n), short-circuit current (I_{SC}), current transformer ratio and tap setting of relays as the initial setting of OCRs are tabulated in Table 3. The instantaneous relays were set based on 50% of the short-circuit current at point *F* (Figure 4). R_7 was also set based on 1.25 I_{SC} when the fault occurred in location R_6. It should be noted that R_6 is the backup protection for R_1 - R_5 and R_7 is the backup for R_6.

Figure 9 shows the time-current curves of R_1-R_5 with different values of *TD* when the ASCC operates in mode 1. The multiple currents of R_1-R_5 are shown in Table 4. Based on Figure 9, in order to meet the protective coordination of R_1 to R_5 for mode 1, the modification of *TD* value from '0.5' to '0.4' (for R_2-R_5) and to '0.3' (for R_1) is needed. Figure 10 shows time-current curves of the main and backup protection of R_6 and R_7 in mode 1 of ASCC. To perform the protective

coordination of R_6 and R_7 in mode 1, the modification of their *TD* values to '0.1' and '0.5' respectively is needed. Table 5 lists the modified values of setting parameters of R_6 and R_7 in the three operation modes of ASCC.

Table 3. Values of OCR parameters

| Circuit breaker	I_n (A)	I_{sc} (A)	Current transformer ratio	Tap setting of relay
1	252.11	12560	700/5	3
2	176.48	12560	700/5	2
3	226.9	12560	700/5	3
4	201.69	12560	700/5	3
5	201.69	12560	700/5	3
6	1058.87	12560	1100/5	8
7	157.46	21240	1100/5	1
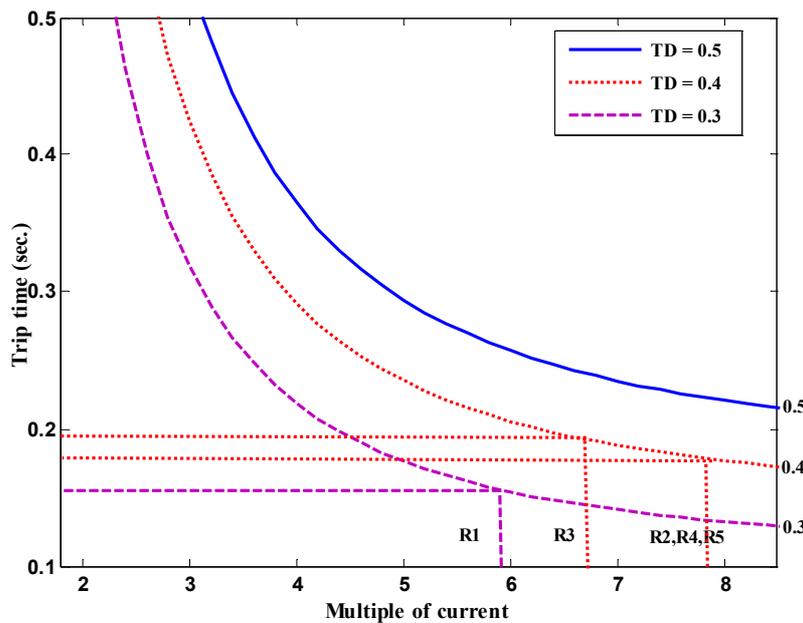
Figure 9. Time-current curves of R_1-R_5 in the case that *TD* is adjusted to meet the coordination in mode 1

According to Tables 4 and 5, if the modifications of *TD* value from '0.5' to '0.3' for R_1 and R_3 and from '0.5' to '0.4' for R_2, R_4 and R_5 are carried out, the protective coordination in mode 2 is achieved. In addition, the coordination of R_6 and R_7 in mode 2 is similar to that in mode 1. Similarly, when the ASCC operates in mode 3, the modification of *TD* value from '0.5' to '0.3' for R_1-R_5 is needed. By the same token, for the coordination of R_6 in mode 3, both setting parameters (*TD* and tap setting) need to be modified. Again, based on Table 5, the modifications of *TD* from '0.7' to '0.1' and also of the tap setting of relay from '7' to '6' are required for R_6. Finally, with the modification of *TD* from '1.7' to '0.4', the coordination of R_7 is done in mode 3.

Table 4. Setting parameters of R_1-R_5 in different modes

			R_1	R_2	R_3	R_4	R_5
Mode1	Without correction	Multiple of current	5.57	7.83	6.71	7.83	7.83
		Trip time (sec.)	0.27	0.22	0.24	0.22	0.22
	With correction	*TD* (sec.)	0.3	0.4	0.4	0.4	0.4
		Trip time (sec.)	0.16	0.18	0.19	0.18	0.18
Mode2	Without correction	Multiple of current	5.43	7.67	5.57	7.67	7.67
		Trip time (sec.)	0.27	0.23	0.27	0.23	0.23
	With correction	*TD* (sec.)	0.3	0.4	0.3	0.4	0.4
		Trip time (sec.)	0.16	0.18	0.16	0.18	0.18
Mode3	Without correction	Multiple of current	4.71	7	5.57	6.5	6.5
		Trip time (sec.)	0.31	0.24	0.27	0.24	0.24
	With correction	*TD* (sec.)	0.3	0.3	0.3	0.3	0.3
		Trip time (sec.)	0.18	0.14	0.16	0.15	0.15
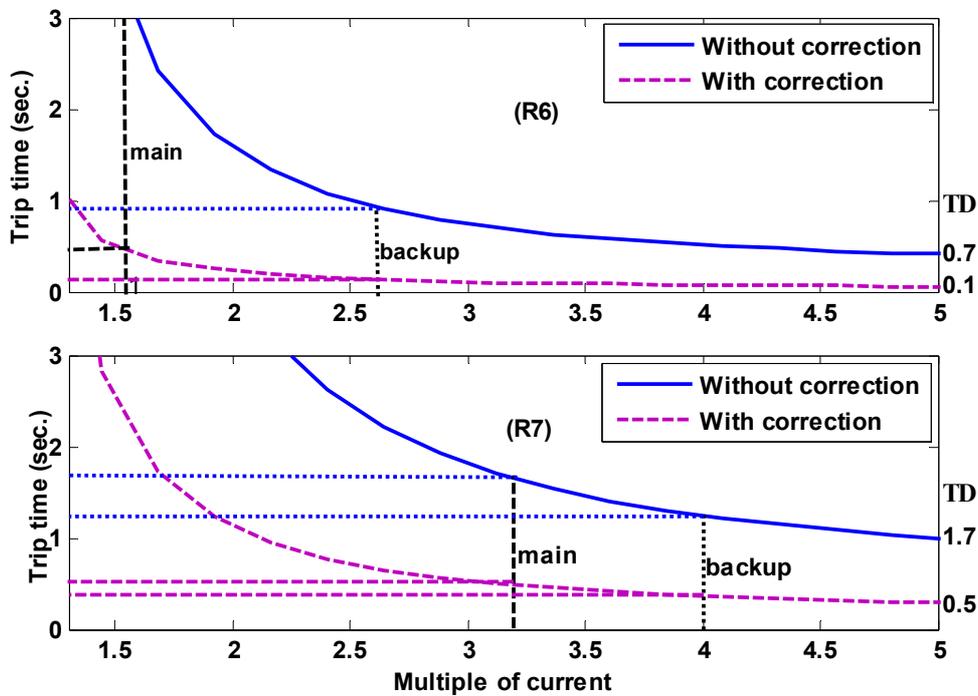
Figure 10. Time-current curves of R_6 and R_7 to meet the coordination of main and backup protection in mode 1

Table 5. Setting parameters of R_6 and R_7 in different modes

		Tap setting of relay	TD	Multiple of current as backup protection	Trip time as backup protection (sec.)	Multiple of current as main protection	Trip time as main protection (sec.)
Mode 1	R_6	7	0.1	1.55	0.59	2.61	0.13
	R_7	1	0.5	3.2	0.53	4	0.36
Mode 2	R_6	7	0.1	1.5	0.58	2.25	0.14
	R_7	1	0.5	3.04	0.54	4	0.36
Mode 3	R_6	6	0.1	1.48	0.58	2.5	0.14
	R_7	1	0.4	2.6	0.54	4	0.3

CONCLUSIONS

When an ASCC was tested through simulations in a typical three-phase circuit to evaluate its effect on fault current limiting, simulation results confirmed the appropriate performance of different operation modes and control strategy of the ASCC. In other words, this study shows that by adjusting the ASCC in different operating modes, the setting parameters of OCRs are modified to obtain the protective coordination. Also, simulation results confirmed that for mode 3, when the amplitude of output current of the converter is increased, the current limiting further decreases. Although ASCC is more effective for current limiting in this case than the other cases, the protective coordination may deteriorate because of an excessive reduction in current even when the OCR parameters are adjusted to their minimum values. Therefore, this limitation should be considered in an ASCC setting.

REFERENCES

1. J. Wang, L. Zhou, J. Shi and Y. Tang, "Experimental investigation of an active superconducting current controller", *IEEE Trans. Appl. Superconduct.*, **2011**, *21*, 1258-1262.
2. K. Kajikawa, K. Kaiho, N. Tamada and T. Onishi, "Magnetic-shield type superconducting fault current limiter with high Tc superconductors", *Elec. Eng. Jap.*, **1995**, *115*, 104-111.
3. I. Shimizu, Y. Naito, I. Yamaguchi, K. Kaiho and S. Yanabu, "Application study of a high-temperature superconducting fault current limiter for electric power system", *Elec. Eng. Jap.*, **2006**, *155*, 20-29.
4. Y. Xin, W. Z. Gong, X. Y. Niu, Y. Q. Gao, Q. Q. Guo, L. X. Xiao, Z. J. Cao, H. Hong, A. G. Wu, Z. H. Li, X. M. Hu, B. Tian, J. Y. Zhang, Y. He, Y. Wang, J. Cui, S. Z. Ding, J. Z. Wang, A. L Ren and F. Ye, "Manufacturing and test of a 35 kV/90 MVA saturated iron-core type superconductive fault current limiter for live-grid operation", *IEEE Trans. Appl. Superconduct.*, **2009**, *19*, 1934-1937.
5. M. Endo, T. Koyama, Y. Takahashi, K. Kaiho and S. Yanabu, "Study of shunt type SFCL equipped with electromagnetic repulsion switch for large capacity" *Elec. Eng. Jap.*, **2010,** *173*, 20-27.
6. L. Chen, Y. J. Tang, J. Shi and Z. Sun, "Simulations and experimental analyses of the active superconducting fault current limiter", *Physica. C. Superconduct.*, **2007**, *459*, 27-32.
7. J. Shi, Y. Tang, L. Chen, J. Wang, L. Ren, J. Li, L. Li, T. Peng and S. Cheng, "The application of active superconducting DC fault current limiter in hybrid AC/DC power supply systems", *IEEE Trans. Appl. Superconduct.*, **2008**, *18*, 672-675.
8. J. Shi, Y. Tang, C. Wang, Y. Zhou, J. Li, L. Ren and S. Chen, "Active superconducting DC fault current limiter based on flux compensation", *Physica. C. Superconduct.*, **2006**, *442*, 108-112.
9. A. Ghafari, M. Razaz and S. G. Seifossadat, "Optimum coordination of overcurrent relays with active superconducting current controller in distribution systems", *J. World. Elec. Eng. Technol.*, **2013**, *2*, 37-43.
10. M. Song, Y. Tang, Y. Zhou, L. Ren, L. Chen and S. Cheng, "Electromagnetic characteristics analysis of air-core transformer used in voltage compensation type active SFCL", *IEEE Trans. Appl. Superconduct.*, **2010**, *20*, 1194-1198.

11. L. Chen, Y. Tang, J. Shi, Z. Li, L. Ren and S. Cheng, "Control strategy for three-phase four-wire PWM converter of integrated compensation type active SFCL", *Physica. C. Superconduct.*, **2010**, *470*, 231-235.

12. L. Chen, Y. J. Tang, J. Shi, N. Chen, M. Song, S. J. Cheng, Y. Hu and X. S. Chen, "Influence of a voltage compensation type active superconducting fault current limiter on the transient stability of power system", *Physica. C. Superconduct.*, **2009**, *469*, 1760-1764.

13. L. Chen, Y. J. Tang, J. Shi, L. Ren, M. Song, S. J. Cheng, Y. Hu and X. S. Chen, "Effects of a voltage compensation type active superconducting fault current limiter on distance relay protection", *Physica. C.Superconduct.*, **2010**, *470*, 1662-1665.

14. J. S. Kim, S. H. Lim and J. C. Kim, "Study on application method of superconducting fault current limiter for protection coordination of protective devices in a power distribution system", *IEEE Trans. Appl. Superconduct.*, **2012**, *22*, 2154-2159.

15. S. H. Lim, J. S. Kim and J. C. Kim, "Analysis on protection coordination of hybrid SFCL with protective devices in a power distribution system", *IEEE Trans. Appl. Superconduct.*, **2011**, *21*, 2170-2173.

16. J. S. Kim, J. F. Moon, S. H. Lim and J. C. Kim, "Study on selection of SFCLs impedance for protective coordination with overcurrent relay in a distribution system", Proceedings of Transmission and Distribution Conference and Exposition: Asia and Pacific, **2009**, Seoul, South Korea, pp.1-4.

17. J. S. Kim, S. H. Lim and J. C. Kim, "Study on protective coordination for application of superconducting fault current limiter", *IEEE Trans. Appl. Superconduct.*, **2011**, *21*, 2174-2178.